Modulated Nanowire Structures for Exploring New Nanoprocessor Architectures and Approaches to Biosensing

Modulated Nanowire Structures for Exploring New Nanoprocessor Architectures and Approaches to Biosensing

A dissertation presented

by

Hwan Sung Choe

to

The Department of Physics

in partial fulfillment of the requirements

for the degree of

Doctor of Philosophy

in the subject of

Physics

Harvard University

Cambridge, Massachusetts

April, 2013

Dissertation Advisor:
Professor Charles M. Lieber

Author:
Hwan Sung Choe

Modulated Nanowire Structures for Exploring New Nanoprocessor Architectures and Approaches to Biosensing

Abstract

For the last decade, semiconducting nanowires synthesized by bottom-up methods have opened up new opportunities, stimulated innovative scientific research, and led to applications in materials science, electronics, optics, and biology at the nanoscale. Notably, nanowire building blocks with precise control of size, structure, morphology, and even composition in one, two, and three dimensions can successfully demonstrate high-performance electrical characteristics of field-effect transistors (FETs) and highly sensitive, selective, label-free, real-time biosensors in the fields of nanoelectronics and nano-biosensing, respectively. This thesis has focused on the design, synthesis, assembly, fabrication and electrical characterization of nanowire heterostructures for a proof-of-concept nanoprocessor and morphology-modulated kinked nanowire molecular nanosensor.

Nanoprocessor

Realization of a fully integrated complex circuit such as a nanoprocessor has remained difficult due to issues of assembly and electrical uniformity of nanowire devices. To surmount these obstacles, we have developed a multi-functional nanoprocessor architecture based on

programmable non-volatile nanowire transistor arrays. Ge/Si core/shell NWs synthesized by chemical vapor deposition according to the vapor-liquid-solid mechanism are coupled with a rationally-designed dielectric shell stack based on a charge-trapping mechanism to realize nanowire field-effect transistors (NWFETs) with well-defined and programmable gate responses. Controlled integration of individual NWFETs yields reconfigurable charge-trapping NWFET arrays consisting of 496 functional device nodes, capable of complex logic functions such as full-adder with a maximal voltage gain of 10 and input/output (I/O) matching. Significantly, the same device arrays can be re-programmed to perform diverse functions including full-subtractor, multiplexer, demultiplexer and D-latch. These results represent a significant advance in both complexity and functionality of nanoelectronic circuits built by the bottom-up approach. Moreover, the architecture demonstrated here provides a general and scalable paradigm for a fully-integrated nanoprocessor with computing, memory and addressing capabilities.

Nano-biosensor

The realization of an electrochemical nano-biosensor that is functional in physiological environments seems unlikely to occur soon, due to the challenges posed by the short Debye length in a high ionic strength solution. Furthermore, development of such a nano-biosensor cannot keep pace with growing demands for a point-of-care or *in vivo* biosensor. To overcome these limitations of conventional electrochemical nano-biosensors, the concept of a kinked NWFET synthesized by rational modulation of morphology and dopant concentration is presented here. This chemical/biomolecular probe is considered and investigated here under physiological conditions. Heavily n-doped (n++)/intrinsic (i)/heavily n-doped (n++) silicon

semiconductor nanowire has been synthesized in a probe-like kinked structure, and modified to form an FET device. Based on models of the NWFET's sensitivity in solution and investigation of reliable surface functionalization to immobilize antibodies, the n-type kinked NWFET biosensor has successfully been demonstrated and verified for sensing cancer markers with Enzyme-Linked ImmunoSorbent Assay (ELISA) method in a microfluidic system at low ionic strength. Furthermore, theoretical analysis of a NWFET biosensor operating with high-frequency modulation predicts new opportunities to sense target proteins at high ionic strength, regardless of protein charge. These results imply that a kinked structural NWFET biosensor with high-frequency measurement will allow realization of a future 3D *in vivo* bioprobe for advanced pathology and proteomics in a single cell.

Contents

To my parents, wife, and daughters

Acknowledgements

This dissertation is the result of far more than five years of study. Every single page also reflects my relationships with the many distinguished and inspiring people I have met since joining the Lieber research group. I cherish all their contributions to my development and achievements as a scholar and a scientist.

First and above all, I would like to thank my dissertation advisor Professor Charles M. Lieber for instilling in me what a good scientist is. As a mentor and a scientist, Charlie not only fired my passion, inspiration, and devotion to my research by sharing his vision with me, but constantly encouraged me toward future achievements. He exemplifies for me the virtues necessary to become a great scientist: insightfulness, eagerness, diligence, and creativity. Undoubtedly, his lessons and guidance have helped to correct my weak points and forced me to think more critically. So, thank you, Charlie. I am truly honored to be your student.

I would also like to thank my current committee members Professor Hongkun Park and Professor Adam Cohen and my previous committee member Professor Charles Marcus for their mentorship. Even though there was never enough time for personal conversations, your advice inspired passion and energy, and helped me onward in my graduate school life.

To Dr. Hao Yan and Dr. SungWoo Nam, I'm truly grateful for your cordial help and collaboration during the nanoprocessor project. When I joined the Lieber research group, Hao, then a senior graduate student, willingly gave his time to teach me semiconductor nanowire synthesis and device fabrication. SungWoo was a good friend as well as a good research partner in the nanoprocessor and graphene bioprobe projects. Whenever I encountered problems, a

discussion with him would give me a new idea to address them. Our synergistic collaboration often enabled me to solve tough problems and create new breakthroughs. As a mentor and sounding board, he played an important role in the achievement of the novel programmable complex nanocircuit in this thesis.

I also want to thank my current collaborator Leon Xueliang Liu for his collaboration with me on the 3D *in-vivo* bioprobe project. He is a very smart person who quickly absorbs new information. His tendency to persist in asking questions and "probing" the unknown until he finds a solution has been a constant driving force toward progress. Furthermore, Leon is a great debating partner and friend, so in my work with him one plus one equals more than two. Our close collaboration has led to huge progress toward not only theoretical understanding but also reliable demonstration of the novel structural NWFET biosensor in this thesis.

I would like to thank my office mates Dr. Quan Qing, Dr. Thomas Kempa, Dr. Tzahi Cohen-Karni, Dr. James Cahoon, Dr. Wooyoung Shim, Bobby Day and Max Markin. They all acted at times as friends, mentors, listeners and helpers. Whether I felt happy, sad, or frustrated, they shared my joy, sorrow or frustration and lightened the load. I hope to keep in touch with you guys for the rest of my life.

I also want to thank all of my labmates. In particular, I'm grateful to Dr. Ping Xie, Dr. Xiaojie Duan, Dr. Qihua Xiong, Dr. Hong-Gyu Park, Dr. Won-Il Park, Dr. Yajie Dong, Dr. Bozhi Tian, Dr. Brian Timko, Dr. Xiaocheng Jiang, Zhe Jiang, Ruixuan Gao, Jia Liu, and Tian-Ming Fu for discussion and conversation about everything from scientific topics to private concerns. I very much appreciate all of them for creating a family within the Lieber group.

I would like to thank Dr. Shamik Das and Dr. Jim Klemic of the MITRE Corporation. Shamik proposed practical and useful designs and functions based on nanowire crossbar array circuits. Jim has visited the group to discuss results and suggested measurements for improved device characterization.

I would like to thank our senior research associate Dr. Jinlin Huang. As an experienced scientist and born teacher, he tries to give me and everyone in the group inspiration and tough questions about physical principles. Always my discussions with him force me to think more deeply and strengthen my weak points. I also owe him a huge thank you for teaching me electronics and maintaining/managing our group's instruments.

I would like to thank the lab administrator Kathleen. She is my good listener as well as good mentor. Whenever I had trouble, she advised me and it always made it right.

Finally, my deepest gratitude goes to my family for their unflagging love and support throughout my life; my graduate student life, as well as this dissertation, would simply have been impossible without them. I am indebted to my father and mother, Ki-man Choi and Jung-ha Lee. Lastly, thank you to my lovely wife, Seon Ah Lee, and to my lovely daughters, Emily Eunji Choe and Grace Eunhye Choe. All of you are the reason why I am happy, why I can love, and why I can keep moving forward. Thank you very very much for being with me. I loved you too, in my past life, I love you in this life, and I will love you forever in my next life.

List of Figures

List of Tables

Chapter 1

Introduction

Nanoscience and nanotechnology had their beginnings with the invention of scanning tunneling microscopy (STM) and discovery of fullerenes in the 1980s. Since then, research on nanoscale phenomena has led to significant advances in physics, chemistry, biology and material science. In particular, the emergence of zero-dimensional (0D) structures such as quantum dots, one-dimensional (1D) structures such as carbon nanotubes (CNT), semiconductor nanowires (NW), and two-dimensional (2D) structures such as graphene has enabled not only examination of new optical, electrical, mechanical, and thermal properties based on quantum effects, but also realization of other novel properties never observed in classical systems. For the last decade, 1D semiconductor NWs have fueled intense progress in nanotechnology and nanoscience due to their several unique advantages and characteristics. First, it is possible to design and develop various 1D nanostructures through precise control of size, morphology, structure, and composition in two and three dimensions. Second, controllable material modulation over many length scales and in many directions enables novel multi-functional devices and new nanoscale heterostructures for study of quantum confinement. Third, synthesized NWs can easily be combined with other nanostructures such as quantum dots, nanopores, or graphene to create

next-generation devices. In this chapter, I will provide a brief overview of nanoscience and nanotechnology with an emphasis on the synthesis of NWs and NW heterostructure systems and also on nanowire field-effect transistors (NWFETs) and their applications.

1.1 Overview of nanotechnology and nanoscience

Since Richard Feynman inspired the concept of nanotechnology, [1] scientists have imagined controllable synthesis of structures through direct manipulation of atoms. Nanotechnology and nanoscience deal with understanding and controlling matter at the length scale of approximately 1 to 100 nanometers.[2] Significantly, nanoscale materials present intriguing phenomena not anticipated by classical physics. First, a nanoscale confined structure, whose size approaches the Fermi wavelength of an electron, has quantized energy levels (Fig. 1-1), in contrast to the continuous energy levels of bulk structures.[3] The small number of confined electrons in a nanosystem causes an electronic density of states which is quantized and which corresponds to harmonics of electron wave functions confined to the quantum dot. This unique property leads to applications in homogenous light-emitting diodes (LED),[4] highly efficient solar cells,[5-6] quantum dot biosensors with high fluorescence quantum yields,[7-8] qubits,[9-11] single electron transistors,[12] and high-performance FETs based on 1D NWs[13-14] or NTs.[15] Second, nanostructures have a large surface-area-to-volume ratio (SA:V). Fig. 1-2 demonstrates the dramatic increase of SA:V from the millimeter to nanometer scale in a cubic structure. This trend is significant for nanoscale applications in sensing,[16-17] catalysis,[18] and spectroscopy[19] because higher chemical reactivity may be associated with the higher surface area available to reactions.

Last, the size of nanomaterials is compatible with essential biological structures and this may enable non-invasive *in-situ* biological research.[20] Due to their small size, nanostructures are less likely to disturb cellular metabolism when injected into the cell.[21-25] Furthermore, direct culture of biological systems on nanostructure-based complex templates[26] is possible and relevant for directly probing key nanomaterial-biological interfaces.

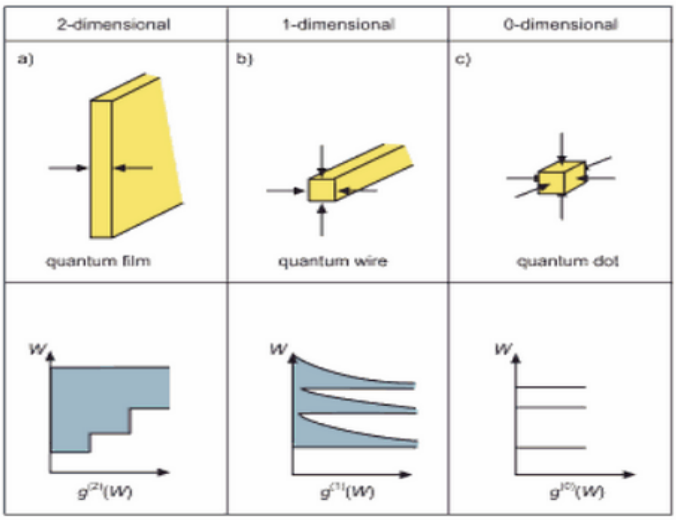


Figure 1-1 Confined structure in 0D, 1D and 2D (from top-right to top-left) and corresponding densities of electron states g(i)(W) (from bottom-right to bottom-left). Courtesy of Ref [3].

To explore and exploit the nano-world, three things are essential: seeing, manipulating, and synthesizing nanoscale matter. Scanning electron microscopy (SEM),[27] tunneling electron microscopy (TEM)[28] and scanning probe microscopy (SPM), including atomic force microscopy (AFM),[27, 29] scanning tunneling microscopy (STM),[30] electrostatic force microscopy (EFM),[31] near-field scanning optical microscopy (NSOM),[32] magnetic resonance force microscopy (MRFM),[33] are generally used to observe and analyze nanostructures. Interestingly, a

combination of STM and AFM techniques allows for observation of morphology and manipulation of atoms (mostly STM) and molecules (e.g. AFM).[34, 35] In addition, strong electric,[36] magnetic,[37] or electromagnetic fields[38] can be implemented in conjunction with the aforementioned techniques to induce specific interactions with nanomaterials. A critical task of nanotechnology and nanoscience is synthesis of nanostructures and nanomaterials in a controllable and reliable manner to yield materials with novel and unique properties. Processes by which nanostructures are produced are largely classified as either "top-down" or "bottom-up." Top-down methods are based on creation of smaller structures or devices by manipulation of a larger material source. Photolithography,[39] e-beam lithography,[40] and dip-pen lithography,[41] followed by etching or deposition of materials, are representative of the top-down process. A key advantage of the top-down approach is that patterning directly defines devices with exquisite alignment and precision. The bottom-up method, on the contrary, relies on synthesis and subsequent organization/assembly of smaller functional components into more complicated structures. Synthesis of quantum dots,[42] nanowires[43-46]/nanotubes,[44, 47] and graphene[48] through chemical deposition is representative of the bottom-up approach. The bottom-up approach offers great flexibility in synthesis and integration to create high-quality homogeneous systems as well as heterogeneous systems with *in-situ* modulation of nanomaterials.[45-46] However, devising methods to self-assemble nanodevice building blocks with high precision and uniformity over large areas remains a significant challenge.

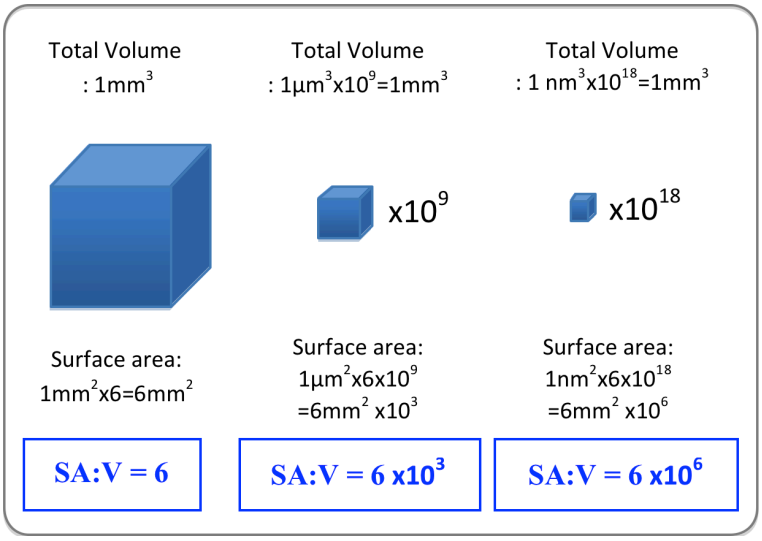


Figure 1-2 Scheme demonstrating the effect of the increased surface area provided by nanostructured materials

The bottom-up method has distinct advantages in the research and application of nanotechnology and nanoscience. In particular, NW research from the bottom-up perspective has the potential for significant impact in nanoelectronics and biosensing. In the next section, I will describe the synthesis of semiconductor nanowires and nanowire heterostructures with precise control of morphology, composition, and electronic properties. Subsequently, I will introduce nanowire field-effect transistors that serve as the basic building blocks for nanoelectronics and nanobiosensors.

1.2 Rational synthesis of semiconductor nanowires and heterostructures

Synthesis of semiconductor nanowire

Nanowires can be grown using electrochemical deposition[49] or chemical vapor deposition (CVD)[43-46] based on a vapor phase mechanism such as vapor-liquid-solid (VLS),[43-46, 50] vapor-solid-solid (VSS),[51-52] oxide-assisted growth (OAG),[53] and self-catalyst growth (SCG).[54] Electrochemical deposition is mainly used for synthesis of metallic nanowires,[49] while CVD is a very common technique for synthesis of semiconductor nanowires.[43-46, 50]

Understanding the VLS mechanism is central to rational synthesis of not only one-dimensional nanowires but also heterostructures. When target atoms of a semiconductor in the **v**apor phase are supplied to a metal nanocluster catalyst at an appropriate growth temperature, the two components will form a eutectic **l**iquid alloy. Once sufficient target atoms supersaturate the metal-semiconductor eutectic alloy, homogeneous nucleation of a single-crystalline one-dimensional **s**olid will begin. The continuous uptake of target semiconductor atoms induces elongation of the nanowire. The nucleation and growth of NWs has been observed by *in-situ* transmission electron microscopy[55]. During synthesis, the nanowire diameter is dictated by metal catalyst size[56] while nanowire length is modulated by growth time. For example, nanowires with ~3 nm diameter ("molecular-scale" nanowires)[57] and millimeter long nanowires[58] have been demonstrated with high controllability and uniformity. Furthermore, switching target atoms capable of eutectic formation with the catalyst enables modulation of material composition during the growth process, making possible the synthesis of superlattices[45, 59]. Furthermore, *in-situ* doping of semiconductor nanowires can be well controlled by the judicious choice of doping material and by control of the dopant feed-in ratio.[59-60]

To choose a suitable metal catalyst and target material for synthesis of semiconductor nanowire the binary phase diagram is consulted. Fig. 1-3a shows the silicon-gold phase diagram.

The diagram depicts distinct phases separated by curves that correspond to non-analytic solutions to the free energy as a function of temperature and percentage of Si atoms. An optimal growth temperature can be found at the intersection of the liquid + metal catalyst and liquid + semiconductor phase boundaries (Fig. 1-3a). In this region, supersaturation can readily occur at low atomic percentages of the target semiconductor. VLS growth entails nucleation and elongation of the nanowire (Fig. 1-3b).

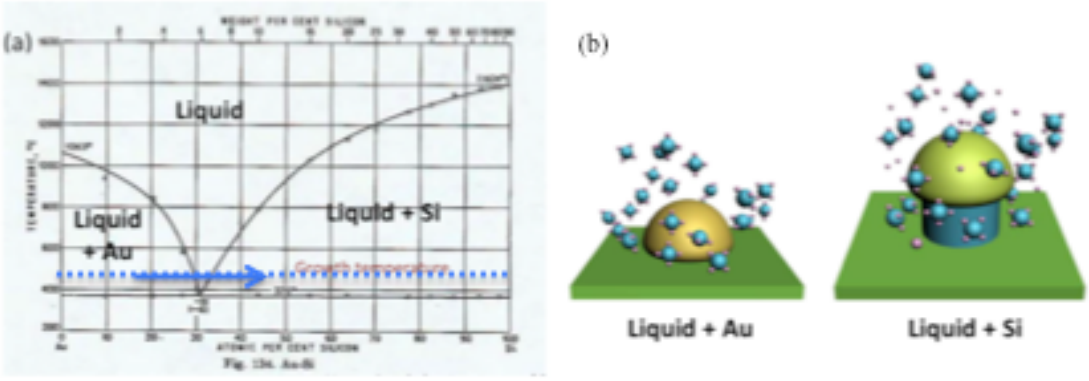


Figure 1-3 VLS mechanism in phase diagram. (a), Liquid-solid phase diagram of Au-Si. Blue arrow corresponds to phase transition in VLS mechanism at growth temperature (blue dashed line). Courtesy of Ref [61]. (b) Schematics of nucleation and elongation in nanowire synthesis by VLS mechanism.

The synthesis of p-type silicon nanowires (p-SiNWs) proceeds as follows. First, a piece of silicon wafer with a top layer of 600 nm silicon oxide (SiO_2) is cleaned with O_2 plasma (100W RF, 1 min at 0.6 Torr) followed by modification with poly-L-lysine (PLL) (0.1% w/v aqueous solution, Ted Pella Inc.) for 10 min. After rinsing with deionized (DI) water, a colloid of 30 nm-diameter Au nanoparticles (Au-NPs) ($2x10^{11}$ particles/ml in water, Ted Pella Inc.) is applied to

the substrate for 10 min and then rinsed off with DI water. Au-NPs disperse and adhere to the PLL-modified growth substrates without aggregation, because Au-NPs in water are negatively charged and thus not only repel each other but also adhere to the positively charged PLL.[62] The catalyst substrate is loaded in the tube-furnace of the CVD system and heated to 460°C. The growth temperature, 460°C, which is higher than the Au-Si eutectic temperature of 370°C, is chosen from the Au-Si phase diagram (Blue dashed line in Fig. 1-3a). To synthesize p-type silicon nanowires with a 4000:1 silicon (Si) to boron (B) ratio (number of boron: 1.5×10^{20} atoms/mol), 2 sccm SiH_4 (100%), and 2.5 sccm B_2H_6 (100ppm in H_2 or He) are introduced into the reactor as precursors for Si and B respectively. Either 60 sccm H_2 or 10 sccm Ar carrier gases are delivered to the catalyst substrate. Total gas pressure is maintained at 40 Torr during growth. After growth for 40 min, nanowires on the substrate are analyzed by SEM and TEM. As shown in Fig. 1-4a, the nanowires are uniform and grown in high yield. Furthermore, high-resolution SEM and TEM images of a single nanowire (Fig. 1-4b) reveal a clear interface between the Au catalyst and Si body at the tip of nanowire.

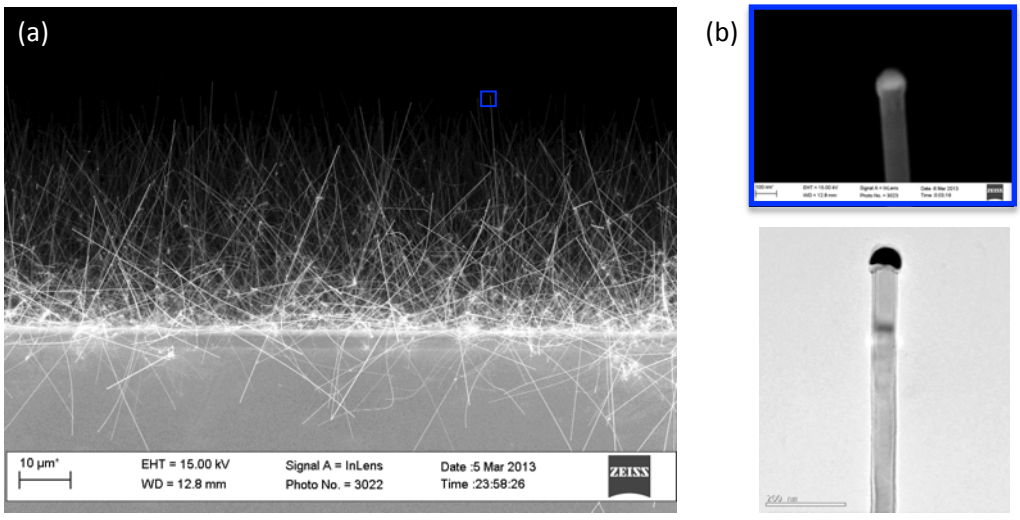


Figure 1.4

Figure 1.4 (Continued)

Figure 1-4 P-type silicon nanowire synthesized by the VLS-CVD method. (a), SEM image of p-type silicon nanowire on the growth substrate. Scale bar: 10 μm. (b), (Upper panel) High-resolution SEM image of one nanowire from image (a). Scale bar: 100 nm. (Lower panel) TEM image of one nanowire transferred from the grown substrate. Scale bar: 200 nm.

Synthesis of core/shell semiconductor nanowire heterostructures

A number of techniques have been developed over the past decades to deposit uniform thin films ranging in thickness from a few monolayers to several micrometers. These techniques can be broadly categorized as physical deposition and chemical deposition.[63] Physical deposition implements mechanical, electromechanical or thermodynamic methods[63]. Chemical deposition, on the other hand, uses precursors that chemically react at the solid surface and leave a solid layer via a vapor-solid (VS) mechanism.[64] The interesting feature of semiconductor nanowire synthesis is that the VLS mechanism entails anisotropic chemical deposition of precursors in only one dimension. However, at different values of temperature (typically higher) and pressure, material precursors decompose in the gas phase or at all nanowire surfaces leading to uniform (radial) deposition of material.

For successful shell growth, chemical deposition must predominate in the radial direction with effective suppression of any axial growth. Typically, either a high temperature and low vapor pressure of precursors,[46, 65] or low temperature (<eutectic) and high vapor pressure of precursors,[46, 66] suffices to suppress axial growth of a nanowire. Under these conditions, the

liquid-solid binary phase diagram has only a liquid phase or solid phase region for both the semiconductor material and catalyst.[61]

The synthesis of intrinsic Si (i-Si)/intrinsic Ge (i-Ge) core/shell nanowires proceeds as follows. The preparation of substrates functionalized with 30 nm Au catalyst is the same as introduced in section 2.1 of this chapter. The catalyst substrate is loaded into a CVD furnace and heated to 465^{o}C for growth of the i-SiNW core. Once the temperature stabilizes, 1 sccm SiH_4 and 60 sccm H_2 are introduced with a total gas pressure of 40 Torr. Growth continues under these conditions for 20 min and is then interrupted by evacuating the reactor and changing the furnace temperature to 330^{o}C for preparation of the i-Ge shell. The growth temperature of 330^{o}C for the i-Ge shell is lower than the eutectic temperature (356^{o}C) of the Ge-Au alloy as shown in Fig 1-5a. After 2 mins at 330^{o}C, 50 sccm GeH_4 (10% concentration) is introduced, and the total gas pressure maintained at 100 Torr for 5 min. TEM images of the nanowire reveal an explicit core/shell nanowire structure with a uniform diameter, in which the core and shell have single-crystalline and amorphous structures, respectively. Under these growth conditions, the shell has growth rate of ~10 nm/min.

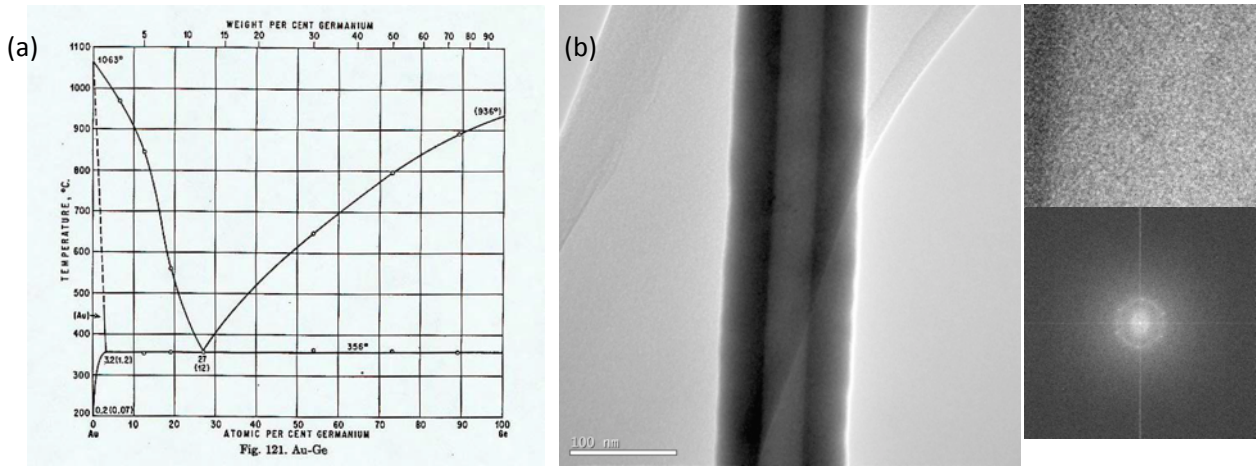


Figure 1.5

Figure 1.5 (Continued)

Figure 1-5 Synthesized i-Si/i-Ge core/shell nanowire with CVD-VLS mechanism. (a), Liquid-solid phase diagram of Au-Ge alloy. Courtesy of Ref [61] (b), (Left panel) TEM image of i-Si/i-Ge core/shell nanowire. Scale bar: 100 nm. (Upper right panel) TEM image of interface between i-Si core and i-Ge shell. Scale bar: 10 nm. (Lower right panel) Fast Fourier transform (FFT) image of i-Si core (upper right panel).

1.3 Semiconductor nanowire field-effect transistor (NWFET)

A semiconductor is a material which has a bandgap on the order of 1 eV, intermediate between that of a metal or an insulator. This small bandgap allows conductivities intermediate between those of insulators and conductors and, more significantly, for the conductivity to be sensitive to temperature, illumination, magnetic field, electric field and impurity atoms. Based on these novel properties, semiconductor materials have been implemented in thermal sensors,[67] photodetectors,[68-70] solar cells,[59, 71-72] magnetic sensors[73] and charge sensors utilizing a p-n junction diode[74] or a transistor.[75]

The transistor has been central to the development of modern electronic systems, including logic and memory, and critical scientific research tools. In particular, the field-effect transistor (FET) has served as the foundation of modern electronics. It is distinguished by an ability to undergo significant conductivity modulation under application of external electric fields, and possesses several other key characteristics. First, the device has a high input impedance, which enables a lower noise intrusion from the environment and less cross-talk from adjacent devices. Second, the size of devices can be scaled down to the molecular level without

significant degradation of performance, because the operation of the device is rooted in the control of the number of majority carriers such as “electrons” or “holes” in the channel.[76] Last, compared to other logic circuits, static power dissipation is very small when two complementary FETs are implemented in a complementary metal-oxide-semiconductor (CMOS) circuit[77].

A semiconductor nanowire field-effect transistor (NWFET) is a molecular-scale analog of a conventional FET and has a number of versatile and powerful functions that can be modulated by rational synthesis. The typical NWFET is composed of four main components (Fig. 1-6a): a semiconducting nanowire, metal contacts, a gate electrode, and an oxide supporting substrate. Two metal electrodes at the edges of the nanowire, a highly conductive electrode positioned in the middle of the nanowire, the nanowire body, and substrate serve as the source/drain, top-gate, channel, and back-gate, respectively. Fig. 1-6a-c shows various top-gate architectures of a NWFET, which can be generally classified as full-top-gate or partial-top-gate structures. These structures share several essential components with conventional metal-oxide-semiconductor field-effect transistors (MOSFETs). As shown in Fig. 1-6b, the MOSFET consists of a p-type semiconductor channel, two heavily n-doped regions for the source and drain, gate electrode, and ohmic-contacted substrate. Three MOSFET performance regimes can be identified depending on the magnitude of the gate-to-source bias (V_{GS}) and drain-to-source bias (V_{DS}):[77] subthreshold, linear, and saturation modes. In the case of most NWFETs, the channel has only one majority carrier and is ohmically contacted with metal electrodes so that there is neither an inversion layer along the channel nor pinch-off in the channel. This means that the NWFET can only operate in two modes such as accumulation mode (channel conductive) for the on-state and depletion mode (channel non-conductive) for the off-state. Significantly, a NWFET with p-n

junction or Schottky contacts for the source and drain[78] reported an inversion mode for lightly doped or intrinsic channels[79]. However, this section will focus on general NWFET mechanisms based on either a full-top-gate or partial-top-gate structure.

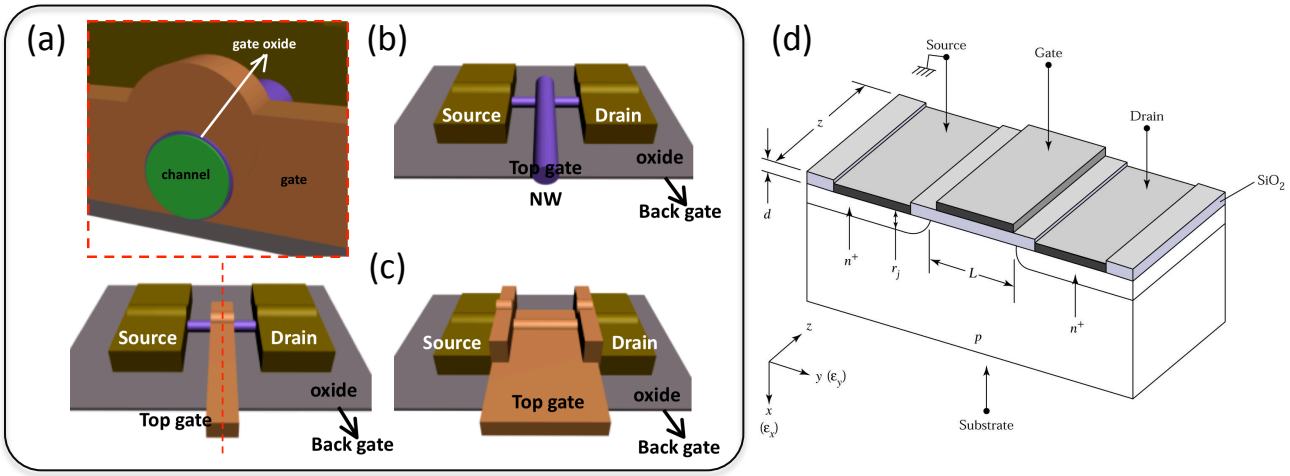


Figure 1-6 FET structures. (a), Scheme of typical NWFET with partial top-gate. (b), Scheme of NWFET with nanowire-based partial top-gate (c), Scheme of NWFET with full top-gate. (d), Scheme of typical MOSFET, showing the channel length ***L****, the channel width* ***Z****, the oxide thickness* ***d****, the junction depth* $\boldsymbol{r_j}$*. Courtesy of Ref [77].*

For a NWFET with a full-top-gate, the drain current in depletion mode (gate voltage below threshold voltage) is dominated by carrier diffusion due to the depletion of majority carriers in the channel. For a p-type NWFET with channel length L, nanowire diameter R, the current can be described as

$$I_{DS} = -q(\pi R^2)D_n \frac{\partial n}{\partial x} = -q(\pi R^2)D_n \frac{n(0) - n(L)}{L} \qquad (1\text{-}1)$$

where D_n is the diffusion constant in the depletion layers, n(x) is the electron density in the channel, and source and drain are at x=0 and x=L. The electron density at the source and drain are given by

$$n(0) = n_i e^{\frac{q(\psi_S - \psi_B)}{kT}}, \quad n(L) = n_i e^{\frac{q(\psi_S - \psi_B - V_D)}{kT}} \tag{1-2}$$

where ψ_S, ψ_B, and ψ_D are the potential at source, nanowire body, and drain, n_i is intrinsic carrier concentration, k is the Boltzmann constant, and T is absolute temperature. Inserting (2) into (1) gives

$$I_{DS} = -q(\pi R^2) D_n \frac{n_i e^{\frac{q(\psi_S - \psi_B)}{kT}} - n_i e^{\frac{q(\psi_S - \psi_B - V_D)}{kT}}}{L}$$

$$= \frac{-q(\pi R^2) D_n n_i e^{\frac{q(\psi_S - \psi_B)}{kT}}}{L} \left(1 - e^{\frac{-qV_D}{kT}}\right) \tag{1-3}$$

Note the exponential dependence of I_D for V_G-V_T < 0. In accumulation mode, where the gate voltage is higher than the threshold voltage, majority carriers induce the conducting channel, such that the channel acts as a resistor. As the drain voltage increases, with the source to gate bias (V_{GS}) maintaining its initial value, the drain to gate bias (V_{GD}) decreases. This effect is referred to as pinch-off and leads to the same operation as in the linear and saturation mode of a conventional MOSFET. The drain currents I_D in the modes[77] are

$$I_{DS} = \frac{1}{L^2} \mu C_{ox} \left((V_G - V_T) V_{DS}\right) \quad for\ V_{DS} \ll (V_G - V_T)\ \ in\ linear\ mode \tag{1-4}$$

$$I_{DS} = \frac{\mu C_{ox}}{2L^2} (V_G - V_T)^2 \qquad for\ V_{DS} \gg (V_G - V_T)\ \ in\ saturation\ mode \tag{1-5}$$

where μ is carrier mobility, C_{ox} is the capacitance of gate oxide, V_G is the gate voltage, V_T is the threshold voltage, and V_{DS} is the drain voltage. The transconductance g_m of the NWFET, which

is an important indicator of electrical device performance, is expressed in different operational modes as

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_G}\right|_{V_{DS}=\,constant} = \frac{1}{L^2}\mu C_{ox} V_{DS} \qquad in\ linear\ mode \tag{1-6}$$

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_G}\right|_{V_{DS}=\,constant} = \frac{1}{L^2}\mu C_{ox}(V_G - V_T) \qquad in\ saturation\ mode \tag{1-7}$$

Fig. 1-7a shows the I_{DS}-V_{DS} plot of a full-top-gate NWFET which demonstrates linear and saturation regions.

For a NWFET with a partial-top-gate geometry, interestingly, there are uncovered, top-gate-free parts of the nanowire between the channel and source/drain contacts. These parts are highly conductive with abundant majority carriers so that the nanowire body does not exhibit pinch-off. Therefore, the source-drain current of a NWFET with a single partial-top-gate in the middle of the semiconductor channel can be expressed in linear mode as follows,

$$I_{DS} = \frac{1}{L^2}\mu C_{ox}\left((V_{GS'} - V_T)V_{D'S'}\right) = \frac{V_{S'} - V_S}{R_{SS'}} = \frac{V_D - V_{D'}}{R_{DD'}} \tag{1-8}$$

where $V_{S'}$ and $V_{D'}$ are the voltage at the interface of the top-gate-free and gate regions close to the source and drain, respectively, $V_{D'S'}$ is the voltage difference in the channel covered by the top-gate, and $R_{SS'}$ and $R_{DD'}$ are the resistance of top-gate-free parts close to source and drain, respectively. Fig. 1-7b shows the I_{DS}-V_{DS} and I_{DS}-V_{GS} curves for a partial-top-gate NWFET which correspond to electrical transport in linear mode.

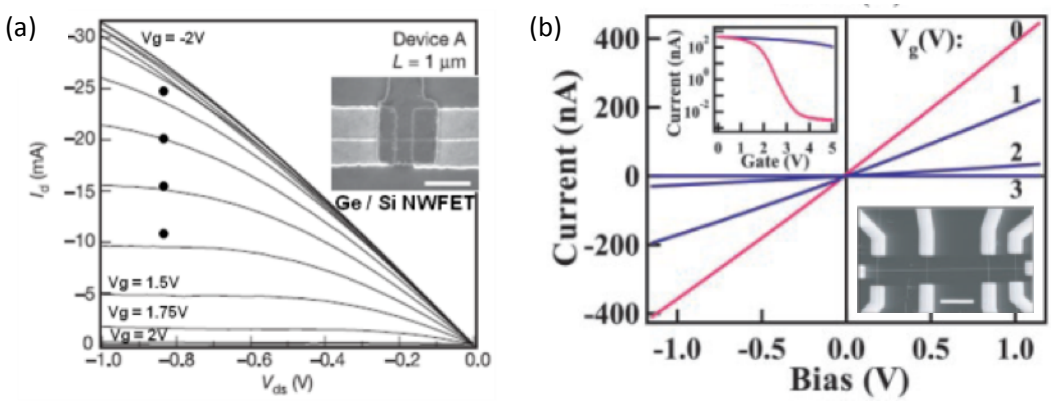


Figure 1-7 Electrical characteristics of NWFET. (a), I_{DS}-V_{DS} data for Ge/Si core/shell nanowire device (L = 1μm, 4 nm HfO_2 dielectric) with V_G = -2 to 2V in 0.25V steps from top to bottom. Inset: Top-view SEM image of the NWFET device. The Au top-gate overlaps with the Ni source/drain electrodes to ensure full coverage of the channel. Scale bar: 500 nm. Courtesy of Ref [13]. (b), Gate-dependent I_{DS}-V_{DS} characteristics of NW-top-gated NWFET. The NW gate voltage for each I_{DS}-V_{DS} curve is indicated (0, 1, 2, and 3V). (Top left inset) The red and blue curves show I_{DS}-V_{GS} for n-type NW (red) and global back-gate (blue) when the bias is set at 1V. (Bottom right inset) SEM image of a multiple crossed NW-top-gated NWFET. Scale bar: 2 μm. Courtesy of Ref [80].

1.4 Organization of thesis

Semiconductor nanowire building blocks coupled with functional materials through bottom-up methods can provide unique properties for use in novel nanoelectronic and nano-biomolecular applications. This thesis studies how to encode new functions into nanowire building blocks through physical design and synthesis and explores new nanoscale architectures for the realization of a nanoprocessor and unique biosensing device.

In part I, Chapters 2-3, we describe how charge-trapping field-effect transistors (CTNWFETs) based on semiconductor/high-*k*-oxide-stack core/shell nanowires were developed, studied, characterized, and assembled to demonstrate reconfigurable multi-functional nanowire circuits for a nanoprocessor. Specifically, chapter 2 describes the bandgap design and development of CTNWFETs through integration of an amorphous shell of a high-*k* oxide stack over single-crystalline semiconductor nanowires using atomic layer deposition (ALD). Furthermore, employing a high-performance Ge/Si core/shell nanowire structure for the core successfully yields enhanced device uniformity, a prerequisite for building complex circuits. In addition, this novel device shows bistable conductance with high ON/OFF ratios ($>10^6$) and can be used for not only logic gates but also memory elements at the nanoscale.

In Chapter 3, we propose a crossbar array architecture consisting of non-volatile CTNWFET as the platform for a programmable integrated nanowire circuit. A simple but effective nanowire assembly method is introduced to enable fabrication of CTNWFET crossbar arrays. A multi-channel electrical measurement system is described. Based on two blocks (one unit tile) of CTNWFET crossbar arrays, we realize a number of complex logic circuits such as NOR, XOR, half-adder, full-adder, full-subtractor, multiplexer, demultiplexer, and D-latch. Furthermore, we demonstrate how this architecture can be scaled to develop a full nanoprocessor system and comment on the low power consumption characteristics of this design.

In part II, Chapters 4-5, we present a novel NWFET biosensor and use this platform to understand the fundamentals of electrically-based biomolecular detection. Critical factors underpinning such detection are explored by means of not only surface modification analysis with X-ray photoelectron spectroscopy (XPS) and contact angle measurement but also enzyme-

linked immunosorbent assays (ELISA). In addition, nanowire biosensing in the high-frequency regime is studied to overcome the limits of charge-based sensing in high ionic strength solutions. In Chapter 4, the theoretical sensitivity of a NWFET biosensor is investigated for design and development of high-sensitivity NWFET through modulation of dopants and morphology in synthesis. The surface modification of a SiNWFET with (3-aminopropyl)triethoxysilane (APTES) and glutaraldehyde (GA), 3-(trimethoxysilyl)butyl aldehyde (TBA), or APTES and N-hydroxysuccinimide (NHS)/1-ethyl-3-(3-dimethylaminopropyl) carbodiimide (EDC) is inspected by XPS and contact angle measurements. Furthermore, ELISA experiments using gold-conjugated secondary antibodies in a microfluidic system reveal ~2000 antibody sites per μm^2 and eventually prove that electrical signal changes from a NWFET biosensor correspond to specific association-dissociation events of charged target proteins.

Finally, in chapter 5, we discuss issues related to the use of electrically-based biosensors and demonstrate a new NWFET-based biosensor in high ionic strength solutions. This biomolecule-sensing nanoelectronic probe has the potential to open up new opportunities in nanoproteomics and help advance nanoelectronic sensing from *in vitro* to *in vivo* studies.

Bibliography

1 Eric, D. *"There's Plenty of Room at the Bottom" (Richard Feynman, Pasadena, 29 December 1959).*

2 *National Nanotechnology Initiative*, www.nano.gov.

3 Waser, R. *Nanoelectronics and information Technology (Advanced Electronic Materials and Novel Devices).* (WILEY-VCH Verlag GmbH & Co. KGaA, 2005).

4 Alivisatos, A. P. Semiconductor clusters, nanocrystals, and quantum dots. *Science* **271**, 933-937 (1994).

5 Nozik, A. J. Quantum dot solar cells. *Physica E* **14**, 115-120 (2002).

6 Semonin, O. E., Luther, J. M., Choi, S., Chen, H., Gao, J., Nozik, A. J. & Beard, M. C. Peak external photocurrent quantum efficiency exceeding 100% via MEG in a quantum dot solar cell. *Science* **334**, 1530-1533 (2011).

7 Medintz, I. L., Clapp, A. R., Mattoussi, H., Goldman, E. R., Fisher, B. & Mauro, J. M. Self-assembled nanoscale biosensors based on quantum dot FRET donors. *Nature Mater.* **2**, 630-638 (2003).

8 Medintz, I. L., Uyeda, H. T., Goldman, E. R. & Mattoussi, H. Quantum dot bioconjugates for imaging, labeling and sensing. *Nat. Mater.* **4**, 435-446 (2005).

9 Hu, Y., Churchill, H. O. H., Reilly, D. J., Xiang, J., Lieber, C. M. & Marcus, C. M. A Ge/Si heterostructure nanowire-based double quantum dot with integrated charge sensor. *Nature Nanotechnol.* **2**, 622-625 (2007).

10 Ladd, T. D., Jelezko, F., Laflamme, R., Nakamura, Y., Monroe, C. & O'Brien, J. L. Quantum computers. *Nature* **464**, 45-53 (2010).

11 Hu, Y., Kuemmeth, F., Lieber, C. M. & Marcus, C. M., Hole spin relaxation in Ge/Si core-shell nanowire qubits. *Nature Nanotechnol.* **7**, 47-50 (2012).

12 Kastner, M. A. The single electron transistor. *Rev. Mod. Phys.* **64**, 849-858 (1992).

13 Xiang, J., Lu, W., Hu, Y., Wu, Y., Yan, H. & Lieber, C. M. Ge/Si nanowire heterostructures as high-performance field-effect transistors. *Nature* **441**, 489-493 (2006).

14 Jiang, X., Xiong, Q., Nam, S., Qian, F., Li, Y. & Lieber, C. M. InAs/InP radial nanowire heterostructures as high electron mobility devices. *Nano Lett*. **7**, 3214-3218 (2007).

15 Javey, A., Guo, J., Wang, Q., Lundstrom, M. & Dai, H. Ballistic carbon nanotube field-effect transistor. *Nature* **424**, 654-657 (2003).

16 Patolsky, F., Zheng, G., Hayden, O., Lakadamyali, M., Zhuang, X. & Lieber, C. M. Electrical detection of single viruses. *Proc. Natl. Acad. Sci. USA* **101**, 14017-14022 (2004).

17 Zheng, G., Patolsky, F., Cui, Y., Wang, W. U. & Lieber, C. M. Multiplexed electrical detection of cancer markers with nanowire sensor arrays. *Nature Biotechnol.* **23**, 1294-1301 (2005).

18 Yi, D., Lee, S. & Ying, J. Y. Synthesis and applications of magnetic nanocomposite catalysts. *Chem. Mater.* **18**, 2459-2461 (2006).

19 Gammon, D., Brown, S. W., Snow, E. S., Kennedy, T. A., Katzer, D. S. & Park, D. Nuclear spectroscopy in single quantum dots: Nanoscopic Raman scattering and nuclear magnetic resonance. *Science* **277**, 85-88 (1997).

20 Ferrari, M. Cancer nanotechnology: opportunities and challenges. *Nature Rev. Cancer* **5**, 161-171 (2005).

21 Patolsky, F., Timko, B. P., Yu, G., Fang, Y., Greytak, A. B., Zheng, G. & Lieber, C. M. Detection, stimulation, and inhibition of neuronal signals with high-density nanowire transistor arrays. *Science* **313**, 1100-1104 (2006).

22 Tian, B., Cohen-Karni, T., Qing, Q., Duan, X., Xie, P., & Lieber, C. M. Three-dimensional, flexible nanoscale field-effect transistors as localized bioprobes. *Science* **329**, 831-834 (2010).

23 Duan, X., Gao, R., Xie, P., Cohen-Karni, T., Qing, Q., Choe, H., Tian, B., Jiang, X. & Lieber, C. M. Intracellular recordings of action potentials by an extracellular nanoscale field-effect transistor. *Nature Nanotechnol*. **7**, 174-179 (2012).

24 Gao, R., Strehle S., Tian, B., Cohen-Karni, T., Xie, P., Duan, X., Qing, Q. & Lieber, C. M. Outside looking in: Nanotube transistor intracellular sensors. *Nano Lett.* **12**, 3329-3333 (2012).

25 Shalek, A. K., Gaublomme, J. T., Wang, L., Yosef, N., Chevrier, N., Anderson, M. S., Robinson, J. T., Pochet, N., Neuberg, D., Gertner, R. S., Amit, I., Brown, J. R., Hacohen, N., Regev, A., Wu, C. J. & Park, H. Nanowire-mediated delivery enables functional interrogation of primary immune cells: Application to the analysis of chronic lymphocytic leukemia. *Nano Lett*. **12**, 6498-6504 (2012).

26 Tian, B., Liu, J., Dvir, T., Jin, L., Tsui, J. H., Qing, Q., Suo, Z., Langer, R., Kohane, D. S. & Lieber, C. M. Macroporous nanowire nanoelectronic scaffolds for synthetic tissues. *Nature Mater.* **11**, 986-994 (2012).

27 Crawford, S. A., Higgins, M. J., Mulvaney, P. & Wetherbee, R. Nanostructure of the diatom frustule as revealed by atomic force and scanning electron microscopy. *J. Phycol.* **37**, 543-554 (2001).

28 Wang, Z. L. Transmission electron microscopy of shape-controlled nanocrystals and their assemblies. *J. Phys. Chem. B* **104**, 1153-1175 (2000).

29 Binnig, G., Quate, C. F. & Gerber, Ch. Atomic Force Microscope. *Phys. Rev. Lett.* **56**, 930-933 (1986).

30 Shen, T. C., Hubacek, J. S., Tucker, John R. & Abeln, G. C. Nanoscale patterning and oxidation of H−passivated Si (100)-2x1 surfaces with an ultrahigh vacuum scanning tunneling microscope. *Appl. Phys. Lett.* **64**, 2010-2012 (1994).

31 Barboza, A. P. M., Gomes, A. P., Archanjo, B. S., Araujo, P. T., Jorio, A., Ferlauto, A. S., Mazzoni, M. S. C., Chacham, H. & Neves, B. R. A. Deformation induced semiconductor-metal transition in single wall carbon nanotubes probed by electric force microscopy. *Phys. Rev. Lett.* 100, 256804 (2008).

32 Dürig, U. T., Pohl D. W. & Rohner, F. Near-field optical-scanning microscopy. *J. Appl. Phys.* **59**, 3318-3327 (1986).

33 Rugar, D., Budakian, R., Mamin, H. J. & Chui, B. W. Single spin detection by magnetic resonance force microscopy. *Nature* **430**, 329-332 (2004).

34 Snow, E. S., Campbell, P. M. Fabrication of Si nanostructures with an atomic force microscope. *Appl. Phys. Lett.* **64**, 1932-1934 (1994).

35 Sugimoto, Y., Pou, P., Custance, O., Jelinek, P., Abe, M., Perez, R. & Morita, S. Complex patterning by vertical interchange atom manipulation using atomic force microscopy. *Science* **322**, 413-417 (2008).

36 Kim, P. & Lieber, C. M. Nanotube nanotweezers. *Science* **286**, 2148-2150 (1999).

37 Hancox, C. I., Doret, S. C., Hummon, M. T., Luo, L. & Doyle, J. M. Magnetic trapping of rare-earth atoms at millikelvin temperatures. *Nature* **431**, 281-284 (2004).

38 Chaumet, P. C., Rahmani, A. & Nieto-Vesperinas, M. Optical trapping and manipulation of nano-objects with an apertureless probe. *Phys. Rev. Lett.* **88**, 123601 (2002).

39 Sundaramurthy, A., Schuck, P. J., Conley, N. R., Fromm, D. P., Kino, G. S. & Moerner, W. E. Toward nanometer-scale optical photolithography: Utilizing the near-field of bowtie optical nanoantennas. *Nano Lett.* **6**, 355-360 (2006).

40 Craighead, H. G., Howard, R. E., Jackel, L. D. & Mankiewich, P. M. 10-nm linewidth electron beam lithography on GaAs. *Appl. Phys. Lett.* **42**, 38-40 (1983).

41 Piner, R. D., Zhu, J., Xu, F., Hong, S. & Mirkin, C. A. "Dip-pen" nanolithography. *Science* **283**, 661-663 (1999).

42 Klimov, V. I., Mikhailovsky, A. A., Xu, S., Malko, A., Hollingsworth, J. A., Leatherdale, C. A., Eisler, H. J. & Bawendi, M. G. Optical gain and stimulated emission in nanocrystal quantum dots. *Science* **290**, 314-317 (2000).

43 Morales, A. M. & Lieber, C. M. A laser ablation method for the synthesis of crystalline semiconductor nanowires. *Science* **279**, 208-211 (1998).

44 Hu, J., Ouyang, M., Yang, P., & Lieber, C. M. Controlled growth and electrical properties of heterojunctions of carbon nanotubes and silicon nanowires. *Nature* **399**, 48-51 (1999).

45 Gudiksen, M. S., Lauhon, L. J., Wang, J., Smith, D. & Lieber, C. M. Growth of nanowire superlattice structures for nanoscale photonics and electronics. *Nature* **415**, 617-620 (2002).

46 Lauhon, L. J., Gudiksen, M. S., Wang, D. & Lieber, C. M. Epitaxial core-shell and core-multi-shell nanowire heterostructures. *Nature* **420**, 57-61 (2002).

47 José-Yacamán1, M., Miki−Yoshida, M., Rendón, L. & Santiesteban, J. G. Catalytic growth of carbon microtubules with fullerene structure. *Appl. Phys, Lett.* **62**, 657 (1993).

48 Kim, K., Zhao, Y., Jang, H., Lee, S., Kim, J., Kim, K., Ahn, J., Kim, P., Choi, J. & Hong, B. Large-scale pattern growth of graphene films for stretchable transparent electrodes. *Nature* **457**, 706-710 (2009).

49 Sun, L., Searson, P. C. & Chien, C. L. Electrochemical deposition of nickel nanowire arrays in single-crystal mica films. *Appl. Phys. Lett.* **74**, 2803-2805 (1999).

50 Duan, X. & Lieber, C. M. General synthesis of compound semiconductor nanowires. *Adv. Mat.* **12**, 298-302 (2000).

51 Kodambaka, S., Tersoff, J., Reuter, M. C. & Ross, M. F. Germanium nanowire growth below the eutectic temperature. *Science* **316**, 729-732 (2007).

52 Cohen-Karni, T., Casanova, D., Cahoon, J., Qing, Q., Bell, D. & Lieber, C. M. Synthetically-encoded ultrashort-channel nanowire transistors for fast, point-like cellular signal detection. *Nano Lett.* **12**, 2639-2644 (2012).

53 Zhang, R., Lifshitz, Y. & Lee, S. Oxide-assisted growth of semiconducting nanowires. *Adv. Mater.* **15**, 635-640 (2003).

54 Mandl, B., Stangl, J., Hilner, E., Zakharov, A. A., Hillerich, K.,Dey, A. W., Samuelson, L., Bauer, G., Deppert, K. & Mikkelsen, A. Growth mechanism of self-catalyzed group III−V nanowires. *Nano Lett.* **10**, 4443-4449 (2010).

55 Wu, Y. & Yang, P. Direct observation of vapor-liquid-solid nanowire growth. *J. Am. Chem. Soc.* **123**, 3165-3166 (2001).

56 Cui, Y., Lauhon, L. J., Gudiksen, M. S., Wang, J. & Lieber, C. M. Diameter-controlled synthesis of single-crystal silicon nanowires. *Appl. Phys. Lett.* **78**, 2214-2216 (2001).

57 Wu, Y., Cui, Y., Huynh, L., Barrelet, C. J., Bell, D. C. & Lieber, C. M. Controlled growth and structures of molecular-scale silicon nanowires. *Nano Lett.* **4**, 433-436 (2004).

58 Park, W. I., Zheng, G., Jiang, X., Tian, B. & Lieber, C. M. Controlled synthesis of millimeter-long silicon nanowires with uniform electronic properties. *Nano Lett.* 8, 3004-3009 (2008).

59 Kempa, T. J., Tian, B., Kim, D. R., Hu, J., Zheng, X. & Lieber, C. M. Single and tandem axial p-i-n nanowire photovoltaic devices. *Nano Lett.* **8**, 3456-3460 (2008).

60 Xu, L., Jiang, Z., Qing, Q., Mai, L., Zhang, Q. & Lieber, C. M. Design and synthesis of diverse functional kinked nanowire structures for nanoelectronic bioprobes. *Nano Lett.* **13**, 746-751 (2013).

61 Hansen & Anderko, *Constitution of Binary Alloys*, p. 206 & p.232 (1958).

62 Murthy, V. S., Cha, J. N., Stucky, G. D. & Wong, M. S. Charge-driven flocculation of poly(L-lysine) – Gold nanoparticle assemblies leading to hollow microspheres. *J. Am. Chem. Soc.* **126**, 5292-5299 (2004).

63 Seshan, K. *Handbook of Thin film Deposition Processes and Techniques* (Noyes, 2002).

64 Masaki, Y., LeComber, P. G & Fitzgerald, A. G. Solid phase crystallization of thin films of Si prepared by plasma-enhanced chemical vapor deposition. *J. Appl. Phys.* **74**, 129-134 (1993).

65 Tian, B., Zheng, X., Kempa, T. J., Fang, Y., Yu, N., Yu, G., Huang, J. & Lieber, C. M. Coaxial silicon nanowires as solar cells and nanoelectronic power sources. *Nature* **449**, 885-890 (2007).

66 Ben-Ishai, M. & Patolsky, F. A route to high-quality crystalline coaxial core/multishell Ge@ Si (GeSi) n and Si@(GeSi) n nanowire heterostructures. *Adv. Mater.* **22**, 902-906 (2010).

67 Krummenacher, P. & Oguey, H. Smart temperature sensor in CMOS technology. *Sensors. Actuat. A-Phys.* **22**, 636-638 (1989).

68 Cleland, A. N., Estève, D., Urbina, C. & Devoret, M. H. Very low noise photodetector based on the single electron transistor. *Appl. Phys. Lett.* **61**, 2820-2822 (1992).

69 Wang, J., Gudiksen, M. S., Duan, X., Cui, Y. & Lieber, C. M. Highly polarized photoluminescence and photodetection from single indium phosphide nanowires. *Science* **293**, 1455-1457 (2001).

70 Yang, C., Barrelet, C. J., Capasso, F. & Lieber, C. M. Single p-type/intrinsic/n-type silicon nanowires as nanoscale avalanche photodetectors. *Nano Lett.* **6**, 2929-2934 (2006).

71 Chapin, D. M., Fuller, C. S. & Pearson, G. L. A new junction photocell for converting solar radiation into power. *J. Awl. Phys.* **25**, 676-677 (1954).

72 Kempa, T., Day, R., Kim, S., Park, H., & Lieber, C. M. Semiconductor nanowires: A platform for exploring limits and concepts for nano-enabled solar cells. *Energy Environ. Sci.* **6**, 719-733 (2013).

73 Vinal, A. W. & Masnari, N. A. Operating principles of bipolar transistor magnetic sensors. *IEEE Trans. Electron Devices* **2**, 1219-1226 (1994).

74 Chase, F. H., Hamilton, B. H. & Smith, D. H. Transistors and junction diodes in telephone power plants. *Bell Syst. Tech. J.* **33**, 827-858 (1954).

75 Bardeen, J. & Brattain, W. H. The transistor, a semi-conductor triode. *Phys. Rev.* **74**, 230-231 (1948).

76 Cao, L., Chen, S., Wei, D., Liu, Y., Fu, L., Yu, G., Liu, H., Liu, X. & Wu, D. Fabrication and characterization of molecular scale field-effect transistors. *J. Mater. Chem.* **20**, 2305-2309 (2010).

77 Sze, S. M. & Lee, M.-K. *Semiconductor Devices: Physics and Technology* (John Wiley & Sons, 2002).

78 Schmidt, V., Riel, H., Senz, S., Karg, S., Riess, W. & Gçsele, U. Realization of a silicon nanowire vertical surround-gate field-effect transistor. *Small* **2**, 85-88 (2006).

79 Hayden, O., Bjçrk, M. T., Schmid, H., Riel, H., Drechsler, U., Karg, S. F., Lçrtscher, E. & Riess, W. Fully depleted nanowire field-effect transistor in inversion mode. *Small* **3**, 230-234 (2007).

80 Huang, Y., Duan, X., Cui, Y., Lauhon, L., Kim, K. & Lieber, C. M. Logic gates and computation from assembled nanowire building blocks. *Science* **294**, 1313-1317 (2001).

Part I : Programmable multi-functional nanowire array circuit for nanoprocessor

Chapter 2

Design, synthesis, and characterization of non-volatile NWFET for nanoprocessor building block

Conventional CMOS technology has led the nanoelectronic industry for several decades and has altered lifestyles in modern society. However, as devices approach their physical limits in size and as power consumption surges with an increase of transistors,[1] a paradigm shift will be needed to contend with dramatic increases in manufacturing costs. Field-effect transistor (FET) devices based on semiconducting nanowires produced by bottom-up methods are good candidates for nanoelectronic building blocks due to their relative ease of modulation for multiple functions at the nanoscale,[2-4] low-power consumption,[5] and excellent electrical performance.[6, 7] The ability to modulate diameter size, nanomaterial type and electrical properties (by doping) presents new opportunities to produce diverse functional building blocks for nanoelectronics through intelligent design of nanowire structure. This chapter starts with a discussion of NWFETs as the building blocks of electronic applications and addresses design, synthesis, and characterization of novel non-volatile charge-trapping NWFET for the realization of integrated complex circuits in nanoelectronics.

2.1 NWFET for nanoelectronics

An essential factor in electronics is uniform performance between circuit units in terms of threshold voltage and on/off currents, which is one of the critical reasons CMOS technology based on top-down methods has been highly successful. As device features scale down to the sub-100 nm regime, uniformity is key to the success of the device; enormous resources are expended by top-down technology on lithography equipment and operating facilities to minimize fluctuations in device characteristics.[1]

Using nanostructures to assemble devices from the bottom up, analogous to the way that nature builds biological systems,[8, 9] is a possible solution to the problem of maintaining uniformity. Hence, for the past two decades, carbon nanotubes (CNTs)[10, 11] and semiconductor nanowires[12-17] have been investigated and implemented in logic and memory for integrated complex circuits. Their unique controllability in terms of material, structure and impurities[18-21] makes semiconductor nanowires the more promising of these two types of materials for nanoelectronics. Compared to materials produced by top-down methods, the self-assembled semiconducting nanowire guarantees high electrical performance due to single crystallinity with smooth surface boundaries.[22, 23]

For this reason, many researchers have attempted to build complex logic and high capacity memory using semiconducting nanowire building blocks or, more specifically, the NWFET platform. NWFET-nanowire crossbar arrays have successfully demonstrated 'OR,' 'AND,' 'NOR,' 'XOR,' 'half-adder' logic gates,[13] 2 by 2 decoder,[15] ring oscillator,[16, 17] bipolar transistor,[14] CMOS circuit,[14,17] and non-volatile memory.[12] Surprisingly, although a decade has passed since the introduction of functional NWFETs for logic and memory building blocks, one

of the most complex circuits utilizing NWFET building blocks in the history of nanoelectronics is the 2 by 2 decoder. This fact speaks to the significant challenges of high-density integrated complex circuits. These challenges include 1) how to solve variations in device characteristics, 2) which architecture is best to enable complex functionality and 3) how to assemble the individual components in high-density circuits on a large scale.[24] To address these issues and realize integrated multi-functional complex NWFET circuits, in this chapter and the following one we have demonstrated non-volatile NWFET with highly uniform electrical performance capable of both logic and memory functions, a new architecture consisting of a cascade multiple 2D nanowire crossbar array, and a lubricant-assisted contact printing method capable of axial alignment with control of NW density.

2.2 Physical design of charge-trapping NWFET as logic and memory elements

In attempting to realize a complex circuit based on a one-dimensional structure, crossbar array architecture presents itself as an obvious way to achieve not only high device density but also efficient interconnection.[25] However, if all junctions in the crossbar have NWFET functions, it is impossible to demonstrate logic gates, because each row or column in the crossbar array shares the same potential. To address this issue, we consider a bistable NWFET that can achieve two states of an electrical property, FET or highly conductive junction. This concept has been successfully realized by non-volatile NWFET through a surface coating of redox active molecules, cobalt phthalocyanine (CoPc),[12] though it falls short of controllability of electrical properties, such as threshold voltages or on/off currents between devices. We reasoned that the

development of a new multi-state NWFET, with non-volatile, uniform, high on/off ratio electrical performance, is central to achieving integrated complex circuits.

There are two main strategies for conferring non-volatile multi-stable properties on NWFET in which doubling the capacity of stored data and creating multiple bits per cell are feasible. One approach is to couple intrinsic properties of materials, such as ferroelectricity,[26, 27] magnetoresistivity,[28] multiferroicity[29] and phase transition[30, 31] with the NWFET. A second approach is to build a quantum well structure on the NWFET by designing a stack of different dielectrics as a charge-trapping device[32] to control the electron/hole concentration in a confined area. The additional structure on the NWFET would need to play the roles of non-volatility, gate oxide, and multi-stable switching functions simultaneously.

Fig 2-1a-c show a charge-trapping mechanism in which the structure is composed of a tunneling layer, a charge-trapping layer, and a blocking layer. The bandgap energies of the tunneling and blocking layers are much larger than that of the charge-trapping layer, such that joining these heterogeneous materials generates a quantum well where electrons or holes can be trapped. Furthermore, the tunneling layer is designed to be thinner than the blocking layer to make quantum penetration of electrons or holes easy in the tunneling layer and difficult in the blocking layer. Through the quantum tunneling effect, electric charges can pass through the tunneling layer and be trapped in the charge-trapping layer under large bias (Fig 2-1b) on the dielectric stack. Applying a large bias of reverse polarity to the system ejects the trapped charges by the same mechanism.

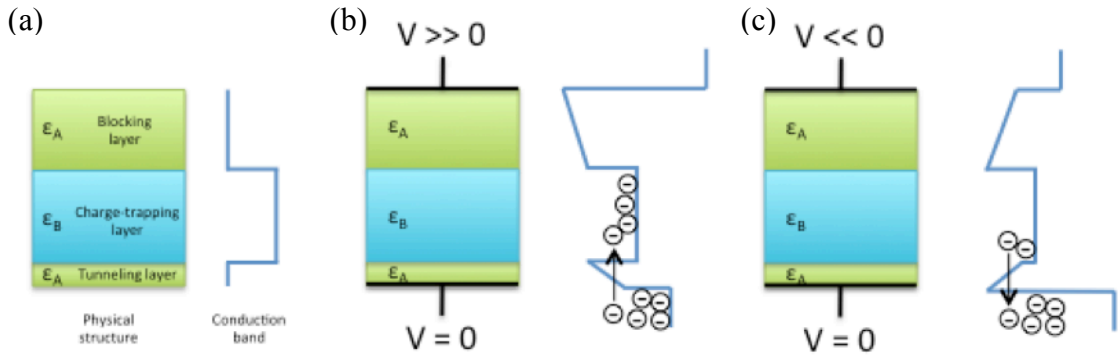


Figure 2-1 Charge-trapping mechanisms. (a), Band structure of a dielectric stack comprising a quantum well, composed of tunneling, charge-trapping, and blocking layers. (b), Applying large positive bias to the dielectric stack. The tunneling effect traps electrons in the middle layer. (c), Applying large negative bias to the dielectric stack. The tunneling effect causes electrons to escape from the charge-trapping layer.

In order to analyze this system quantitatively, a simple simulation of p-type Si/Al_2O_3-ZrO_2-Al_2O_3-ZrO_2-Al_2O_3 30nm/1nm-2nm-1nm-2nm-5nm core/shell NWFET was performed to calculate the threshold shift between the two different NWFET states by the change in hole concentration in the functional gate oxides stack due to charge-trapping. The bandgaps of amorphous alumina, zirconia and silicon dioxide are known to be ~8.8 eV, ~5.8 eV, and ~9 eV,[33] respectively, so that 1nm SiO2, 2nm-1nm-2nm ZrO_2-Al2O_3-ZrO_2, and 5nm Al_2O_3 constitute the tunneling, hole-trapping, and blocking layers, respectively. Fig. 2-2 and Table 2-1 show the physical structure, estimated bandgap structure and parameters of the charge-trapping NWFET for this simulation. In addition, Three features are assumed for the simulation of NWFET: First, this NWFET system assumes that the source and drain contacts are ohmic on the nanowire by

etching through the gate oxides. Second, the shape of the gate metal and oxides is cylindrical. Third, the distribution of dopants is uniform throughout the volume of the NWFET.

Table 2-1 *Parameters of the charge-trapping NWFET* for the simulation

Parameter	**Value**
radius of nanowire core (r_{core})	15 nm
Length of nanowire channel (L)	0.1 μm
Length of nanowire	2.1 μm
Mobility of silicon nanowire (μ_p)	3.65 x 10^2 cm^2 / V· s^{16}
Temperature (T)	300 K

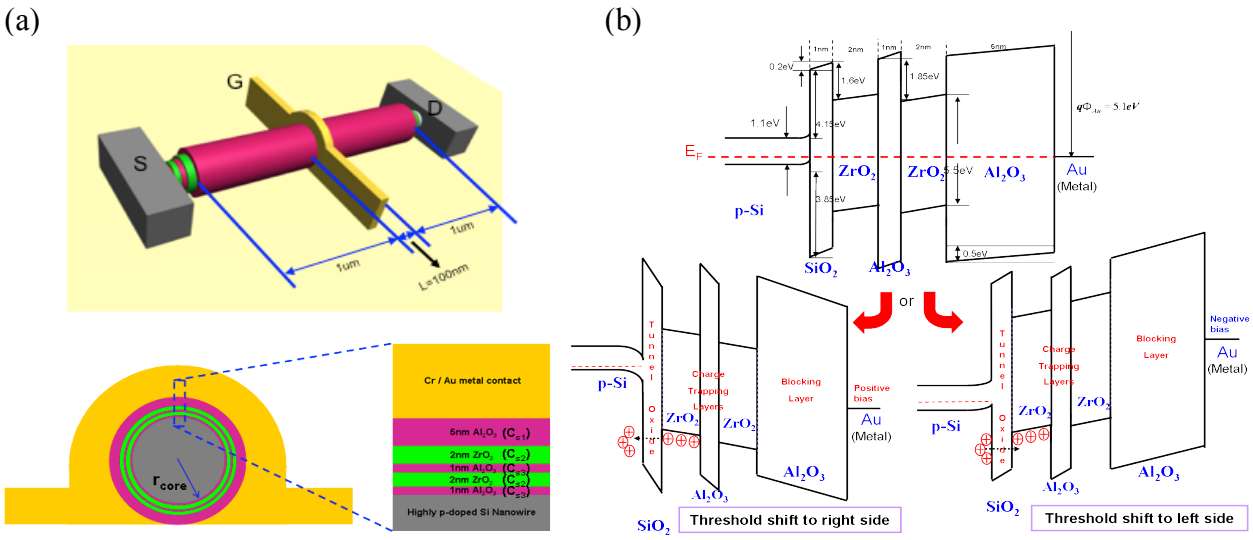


Figure 2-2 Physical and bandgap structure of simulated CTNWFET. (a), Prospective and cross-sectional view of p-type Si/Al2O3-ZrO2-Al2O3-ZrO2-Al2O3 core/shell NWFET with a single partial top-gate. (b), Bandgap structure of 1nm-2nm-1nm-2nm-5nm *Al2O3-ZrO2-Al2O3-ZrO2-Al2O3 multi-dielectric stack. Applying large positive (negative) bias on the top-gate induces the threshold shift to right (left) side.*

To estimate the resistivity of nanowire and boron dopant density, we use the empirical results from p-type SiNW grown with a 4000-to-1 atomic ratio of silicon to boron, 2 μm in length and 30 nm in diameter. The measured conductivity is approximately 5 μS, yielding the resistivity and number of boron atoms in the dopant:

$$\rho = \frac{A}{GL} = \frac{\pi \times (30 \times 10^{-7} cm)^2}{5 \times 10^{-6} S \times 2 \times 10^{-4}\ cm} = 2.8 \times 10^{-2} \Omega \cdot cm$$

$$= \frac{1}{\sigma} = \frac{1}{q\mu_n n + q\mu_p p} \approx \frac{1}{q\mu_p p} \qquad (\because n \ll p)$$

$$\therefore p = \frac{1}{q\mu_p \times 2.8 \times 10^{-2} \Omega \cdot cm}$$

$$= \frac{1}{1.6 \times 10^{-19} C \times 3.65 \times 10^{2} cm^2 \cdot V^{-1} \cdot s^{-1} \times 2.8 \times 10^{-2} \Omega \cdot cm}$$

$$= 6.11 \times 10^{17} cm^{-3} \qquad (2\text{-}1)$$

where ρ, G, σ, p, n, μ_p, and μ_n are resistivity, conductance of nanowire, conductivity, hole concentration, electron concentration, hole mobility, and electron mobility, respectively. The total capacitance of multiple gate dielectrics can be calculated as the serial connection of individual cylindrical capacitors of each oxide layer so that

$$C_{oxide} = \frac{2\pi\varepsilon\varepsilon_0}{ln\left(\frac{t_{ox} + r_{core}}{r_{core}}\right)} \qquad (2\text{-}2)$$

$$C_{total} = \frac{1}{\frac{1}{C_{s1}} + \frac{1}{C_{s2}} + \frac{1}{C_{s3}} + \frac{1}{C_{s2}} + \frac{1}{C_{s3}}} = 2.2 \times 10^{-11} F/cm \qquad (2\text{-}3)$$

where C_{oxide} is the capacitance per length of general cylindrical capacitor which has inside radius r_{core} and outside radius $t_{ox} + r_{core}$, and ε, ε_0, C_{total}, C_{S1}, C_{S2}, and C_{S3} are the dielectric constant, vacuum permittivity, capacitance per length of the total gate oxide stack, of the silicon oxide, of

the aluminum oxide, and of the zirconium oxide, respectively. Because the charge-trapping NWFET is an independent combination of charge-trapping mechanism and three-terminal field-effect switching, transconductance of the NWFET will be calculated in this system first.

As mentioned above, the NWFET is a three-terminal switch modulated by a gate electric field so that the interface between nanowire and gate oxide induces surface dipoles, eventually enhancing or depleting the majority carriers in the nanowire channel. Hence, by introduction of a depletion depth from the surface to the center of nanowire, the transconductance of the NWFET can be calculated. The depletion depth "t_d" can be calculated by solving Poisson's equation as follows.

$$\frac{d^2\phi}{dt^2} = -\frac{q}{\varepsilon_{Si}}(p - n + N_d - N_a) \tag{2-4}$$

where p and n are hole and electron concentration, and N_d and N_a are donor and acceptor density. This equation cannot be solved analytically. Here, employing the depletion approximation[34] which is p = n = 0 (no free charge population) and $N_a >> N_d$, $p << N_a$, at t = td in p-type nanowire, equation (2-4) can be simplified as

$$\frac{d^2\phi}{dt^2} = -\frac{qN_a}{\varepsilon_{Si}} \tag{2-5}$$

which is a solvable form. The solution of equation (2-5) is

$$\phi = \frac{qN_a{t_d}^2}{2\varepsilon_{Si}} + \frac{qN_a t_d \times 2\pi r_{core}}{C_{total}} \quad at\ t = t_d \tag{2-6}$$

$$\Longrightarrow t_d = \frac{2\pi r_{core} \times \varepsilon_{Si}}{C_{total}}\left\{-1 + \sqrt{1 + \frac{2{C_{total}}^2(V_G - V(x))}{qN_a\varepsilon_{Si} \times (2\pi r_{core})^2}}\right\} \tag{2-7}$$

assuming the surface potential on the nanowire along the channel, $V_G - V(x) \cong V_G$. From the depletion depth, the resistance in 100nm NWFET channel can be estimated as

$$R_{ch} = \rho \frac{L}{A} = \rho \frac{L}{\pi(r_{core} - t_d)^2} \tag{2-8}$$

Now, considering the constant resistance r_0 of nanowire except the channel shown in Fig. 2-3a, we can finally solve for the relationship between source-drain current I_{ds} and top-gate voltage V_G by Ohm's law as follows:

$$I_{ds} = \frac{V_{ds}}{2r_0 + R_{ch}} \tag{2-9}$$

$I_{ds} - V_G$ curve is plotted in Fig. 2-3b based on organized equation from inserting equation (2-7) and (2-8) into equation (2-9)

In addition, charge-trapping mechanism can be reflected on the analysis of NWFET by using Fowler-Nordheim (FN) tunneling[35] which is the process whereby electrons tunnel through a barrier by external electric field. The FN tunneling says the tunneling current as

$$J = q v_R \cdot exp\left(-\frac{4}{3} \cdot \frac{\sqrt{2qm}}{\hbar} \cdot l\phi_B\right) \tag{2-10}$$

Therefore, the amount of trapped charge penetrating the barrier and the inducible change of the gate voltage from equation (2-10) are

$$V_{trap} = \frac{Q_{trap}}{C_1} = \frac{J}{C_1 v_R} = \frac{q}{C_1} \cdot exp\left(-\frac{4}{3} \cdot \frac{\sqrt{2qm}}{\hbar} \cdot l\phi_B\right) \tag{2-11}$$

The charge-trapping effect on the NWFET is shown in Fig. 2-3c, which explicitly demonstrates the threshold shift contributed by hole or electron tunneling and shows a sizable hysteresis curve in the $I_{ds} - V_G$ curve.

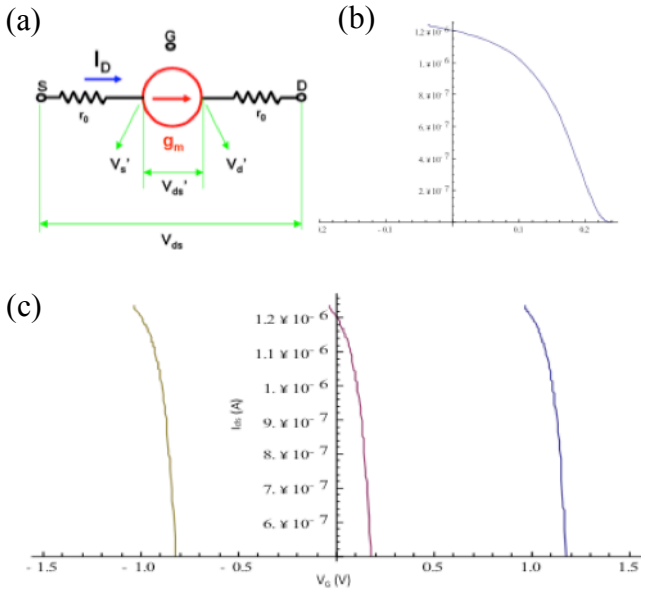


Figure 2-3 Simulation results of NWFET and CTNWFET. (a), Scheme of equivalent circuit of NWFET. (b), Simulation result of NWFET $I_{ds} - V_{ds}$ curve at V_G =0V. (c), Simulation result of NWFET $I_{ds} - V_G$ curves at V_{ds} =1V with V_{trap} =-1V (yellow), 0V (pink), 1V (blue). Note that 1V V_{trap} equals to 6.6 $\times 10^{-9}$C. All graphs are plotted by Wolfram Mathmatica®.

2.3 Fabrication of core/shell NWFET

The fabrication of reliable, high-quality core/shell NWFET with a defect-free high-k shell stack is fundamental to realizing CTNWFET and fully integrated multi-functional nanowire crossbar arrays for complex circuits. In this section, I provide typical methods for fabricating NWFET, and discuss the deposition of the high-k multiple shell structure by atomic layer deposition (ALD).

Nanowire transfer

Nanowire grown by the CVD-VLS method forms a "forest" on the substrate as shown in Fig. 1-4a. These nanowires as synthesized need to be transferred in solution to other substrates such as silicon wafer and flexible Kapton® plastic[36] in order to fabricate NWFET devices. The growth substrate is sonicated in 100% ethanol or isopropanol (IPA) for a few seconds to create a colloidal solution of nanowire (Fig. 2-4a). The solution can be drop-casted onto the marker substrate for registry of the nanowire location. Due to the random positions and orientations of drop-casted nanowires (Fig. 2-4b), this method is not appropriate for making nanowire array structures, but it is the simplest way to fabricate single-NWFET devices. Controllable approaches for nanowire transfer appropriate for realizing crossbar array structure will be discussed in Chapter 3.

(a) (b)

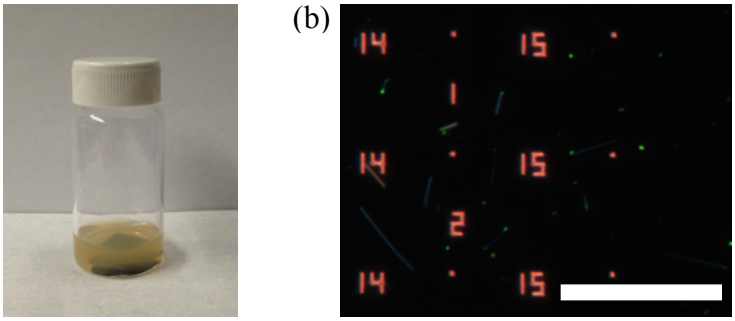


Figure 2-4 SiNW transfer. (a), SiNW colloids in ethanol. (b), Dark-field optical image of drop-casted SiNW on pre-defined marker substrate. Scale bar: 40μm.

Nanowire registration

To fabricate source, drain, and gate for NWFET, metal electrodes must be connected to the nanowire, which means that the nanowires should be registered on pre-patterned markers. High-resolution images of nanowires can be obtained by SEM. However, the process of imaging by SEM involves physical bombardment of high-energy electrons, which can disturb the electrical properties of nanowire. For that reason, a dark-field optical microscope with polarizing filter is often used for the registry of a single nanowire. Interestingly, even though the diameter of nanowire is less than the diffraction limit of visible light, the intensity of scattered light in the dark field is strong enough to see the 1D structure shown in Fig. 2-5a and c, because of its length. Furthermore, comparing the intensities of scattered light from nanowires with SEM image in Fig. 2-5a and b reveals that individual nanowires can be identified by dark-field microscopy, even though the two adjacent nanowires beyond the diffraction limit of the light source cannot be resolved. This approach successfully allows the registration of highly dense nanowire arrays, as in Fig. 2-5c.

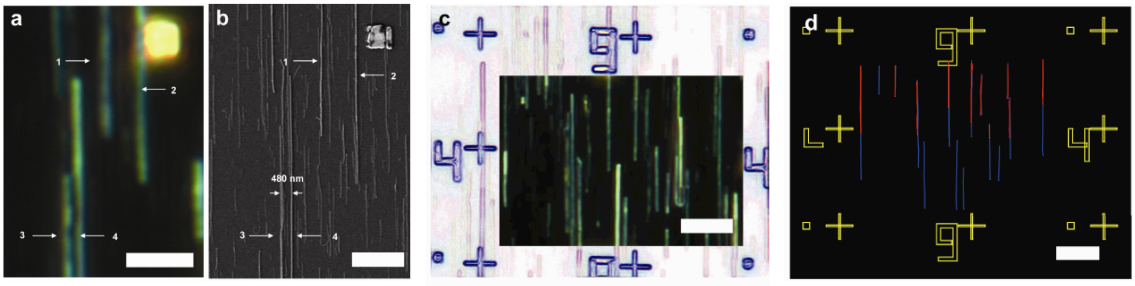


Figure 2-5 Nanowire registration with optical microscope. (a-b), dark-field optical (a) and SEM (b) images of the same region of a 30-nm SiNW array. The corresponding nanowires in (a) and (b) are marked. Note that short and thin nanowires are not revealed in dark-field optical imaging with polarized filter because of small scattering. (c) Optical image of the same region as (a-b) with

Figure 2-5 (Continued) crossbar and number markers. A program automatically registers nanowire and marker position based on highlighting of the edges. (d), Nanowires registered by the program, Igor Pro™, courtesy of Dr. Q. Qing, based on optical (blue) and SEM (red) images. Scale bar: 6 μm.

Electron Beam Lithography (EBL)

EBL is used to pattern electrodes for source, drain, and gate with high resolution and precision on randomly dispersed nanowires. The use of appropriate e-beam resist is important to effect correct resolution, thickness, and negativity/positivity of the patterns. In order to achieve positive patterns with both high resolution and large undercut, polymethyl methacrylate in chlorobenzene (PMMA 950 C2, MicroChem Corp.) and copolymer methylmethacrylate-methacrylic acid (MMA EL9, MicroChem Corp.) have been used were used here.

After drop-casting nanowires onto a marker substrate, the substrate is spin-coated with either PMMA or PMMA/MMA resists at 4000 rpm followed by baking on a hotplate at 180^{o}C for 5 min. This treatment achieves a 100 nm or 500 nm polymer thickness.[37] Next, a ~20 nm conducting polymer (ESPACER, Showa Denko Inc.) is spin-coated on top of the polymer to prevent electrons from accumulating on the surface of both dielectric substrate and semiconducting nanowire during e-beam exposure. EBL is performed with a JSM-7000 (JEOL Ltd.) e-beam writer that is an SEM with a beam blanker. The e-beam acceleration voltage is 30 kV, beam currents are 25 pA and 350 pA for sub-micron and few-micron patterns, and area dosages are 270~380 μC/cm^2 and 350~450 μC/cm^2 for the PMMA and MMA layers. The patterns are rinsed with deionized (DI) water to remove ESPACER, developed in a 1:3 methyl

isobutyl ketone to isopropyl alcohol mixture (1:3 MIBK:IPA, MicroChem Corp.) for 90 s, and rinsed with IPA for 30 s.

Metallization

To fabricate NWFET, metallization processes are necessary to create source, drain and gate. In general, a semiconducting nanowire forms a Schottky barrier at a metal junction as in the case of source and drain metallization[34]. However, the height of a Schottky barrier can be lowered through the choice of appropriate metal so that the contact behaves transparently at room temperature (RT).[38] In order to form ohmic contacts with silicon nanowire, palladium (Pd) and nickel (Ni) are commonly used. Pd can make a transparent contact with SiNW at RT. However, adhesion is poor; thus either thin chromium (Cr) or titanium (Ti) is metallized with Pd for the adhesion layer. Ni, in contrast, cannot form transparent contact with SiNW, so the junction of SiNW and Ni is annealed at high temperature to form nickel silicide (NiSi) which is transparent with SiNW at RT. For the annealing process, rapid thermal annealing (RTA) is commonly used at 300~350^{o}C with forming gas (5% hydrogen in nitrogen).

In practice, most semiconducting materials react in the air to produce native oxides on their surfaces, so that removal of this oxide before metallization with Pd or Ni is critical for the formation of transparent contacts, particularly for source and drain. In the case of silicon dioxide for example, either buffered hydrofluoric acid (BHF) or buffered oxide etchant (BOE), which is a mixture of a buffering agent such ammonium fluoride (NH_4F) and hydrofluoric acid (HF) in water, is commonly used for controllable (slow and constant) etching, in contrast to HF only. The chemical equations for Si etching with HF or BHF are

$$SiO_2 + 6HF \rightleftharpoons 2H^+ + SiF_6^{2-} + H_2O$$

$$SiO_2 + 4HF + 2NH_4F \rightleftharpoons 2NH_4^+ + SiF_6^{2-} + H_2O$$

Note that both reactions produce water, which significantly change the equilibrium constant in the case of HF only. The 1:7 BOE etchant achieves ~1 nm/s etching of SiO_2, so must be used immediately before starting metallization of source and drain[39]. Fig. 2-6 shows the Schottky barrier and the transparent contact of NWFET at RT without and with oxide etching, respectively, before metallization.

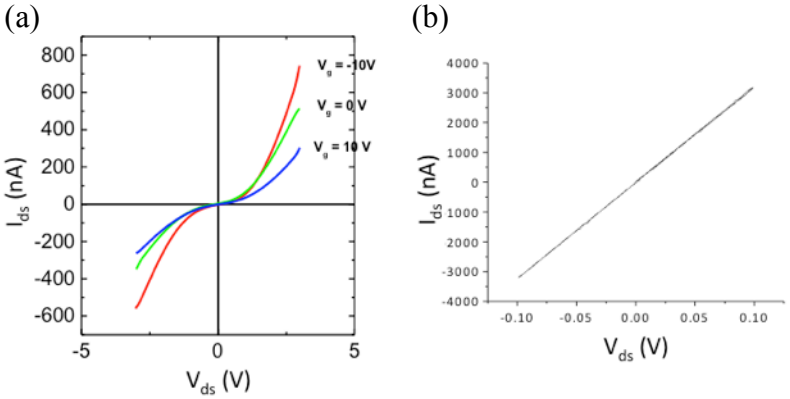


Figure 2-6 Metal-semiconducting nanowire contacts at room temperature. (a), Schottky contact. (b), Ohmic (transparent) contact.

In contrast to source and drain metallization, top-gate metallization forms the junction of a dielectric material and a metal. The work function of the metal plays a role in determining the characteristics of NWFET by shifting the flat-band voltage (VFB).[34] In p-type NWFET including 1D hole gas Ge/Si core/shell NWFET[6], the top-gate metals of low work function shift the threshold voltage (V_{th}) to the left and top-gate metals of high work function shift V_{th} to the right.

Therefore, the NWFET V_{th} can be predictably controlled and tuned by the appropriate selection of metal.

Deposition of high-k oxide shell structure

The most critical aspect of conferring charge-trapping functionality onto the NWFET is deposition of the defect-free high-k dielectric shell structure. One of the best approaches for achieving this is atomic layer deposition (ALD,) which provides excellent conformity and reproducibility by a self-limiting mechanism. Accurate but simple control of deposition thickness at the atomic scale with a wide range of materials is desirable in order to build very thin heterogeneous high-*k* shell structure with sharp interfaces. Details of the ALD mechanism will be discussed in the appendix A.

In order to deposit the shell on a 1D nanowire structure by ALD, two strategies are considered. The first is to stack the shell on the freestanding nanowires in the disordered "forest" on the growth wafer immediately following synthesis. The other is to deposit the shell onto NWFET devices. Fig 2-7a and b illustrate the two strategies. The first approach requires high-k shell etching for the metallization of source and drain to make ohmic contacts, which is a primary cause of low device yields. By contrast, the second approach makes a simple fabrication feasible without the concerns of fabricating reliable contacts. Therefore, the second strategy is adopted here for fabrication of CTNWFET and fully integrated CTNWFET crossbar arrays, as will be demonstrated in the next section and the following chapter.

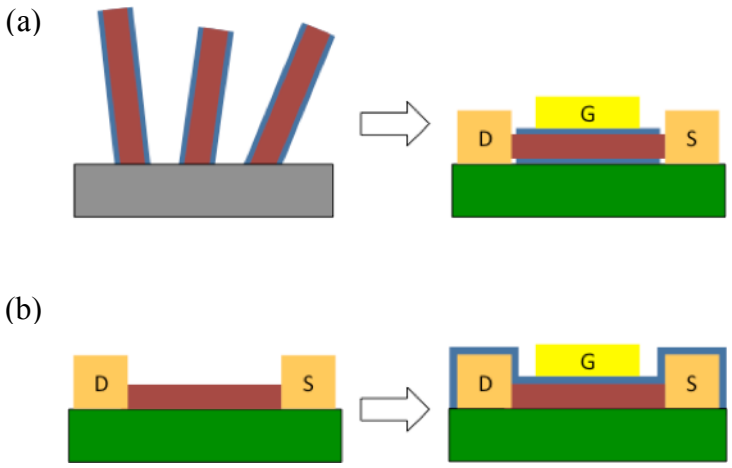


Figure 2-7 Two strategies for the fabrication of shells on NWFET. (a), Core/shell NWFET starting from as-synthesized semiconductor/dielectrics core/shell nanowire. (b), Core/shell NWFET starting from bare semiconductor nanowire, followed by dielectric shell deposition on NWFET by ALD.

2.4 Fabrication and electrical characterization of CTNWFET device

As discussed in section 2-2, a non-volatile bistable NWFET device based on the charge-trapping mechanism can be built in a high-k dielectric shell structure, which is designed to form the band structure of a quantum well by using tunneling, charge-trapping, and blocking layers. To investigate the electrical properties of CTNWFET, a p-type Si/SiO_2-ZrO_2-Al_2O_3-ZrO_2-Al_2O_3 (1nm-2nm-1nm-2nm-5nm) core/shell NWFET is fabricated via the following procedures. The p-type SiNW core is synthesized by the VLS-CVD method to achieve 30 nm diameter and 4000:1 Si:B atomic ratio, followed by annealing of the growth substrate in O_2 at 600^{o}C for 10 min to form a ~1-nm thermal SiO_2 shell which will serve as the tunneling layer. Further shell

deposition with the other oxides is performed by ALD at 300°C with $ZrCl_4$ and trimethyl aluminum (TMA) precursors for ZrO_2 and Al_2O_3 deposition respectively. The as-synthesized Si/SiO_2-ZrO_2-Al_2O_3-ZrO_2-Al_2O_3 (1nm-2nm-1nm-2nm-5nm) core/shell charge-trapping nanowires (CTNWs) are drop-cast onto the Si_3N_4 substrate with pre-defined markers after creating a CTNW colloidal solution by sonication of the growth substrate. Based on registry information obtained for the transferred CTNWs by dark-field optical microscope, EBL is carried out on the PMMA/MMA spin-coated CTNW substrate to define source and drain, followed by development of the e-beam-patterned substrate with 1:3 MIBK:IPA for 90 s and IPA for 30 s. The substrate is etched with 1:7 BHF for 20 s to remove all dielectric shells, and immediately loaded into the thermal evaporator. 1.5 nm/68.5 nm Ti/Pd film are deposited at $2x10^{-7} \sim 6x10^{-7}$ Torr. After lift-off, the second EBL process, using the same conditions as in the first round, is performed to define the single top-gate at the center of the CTNWFET. The 1.5nm/68.5nm Cr/Au film is then deposited for the top-gate by thermal evaporator.

CTNWFET device characteristics

Fig. 2-8a shows the I_{ds}-V_{ds} curves at different top-gate voltages. The device has transparent contacts and shows a linear mode in MOSFET as discussed in Chapter 1-3. Fig. 2-8b shows the conductance-V_G curves. The top-gate sweeping demonstrates a counterclockwise hysteresis curve whose width is related to the absolute value of the applied maximum top-gate voltage. When a large negative bias is applied to the top-gate, the majority carriers, i.e. holes, in the p-type nanowire channel will pass through the 1-nm SiO_2 tunneling layer and be trapped in the ZrO_2-Al_2O_3-ZrO_2 layers, inducing a leftward shift of the threshold voltage. When large

positive bias was applied to the top-gate, a rightward shift is observed. Eventually, these threshold voltage shifts caused by the concentration of trapped holes in the multi-dielectric shell result in counterclockwise hysteresis in the conductance vs. V_G curve, as in Fig 2-8b. Interestingly, wider sweeping of the top-gate voltage causes a wider hysteresis window, which can be attributed to more injected/ejected holes to/from the charge-trapping layer by the higher top-gate bias. It is worth noting that, in the top-gate range of -2 V to 2 V, there are two states where the conductance is different at the same V_G. Furthermore, the two states are non-volatile at 0V top-gate with ~10^7 conductance difference.

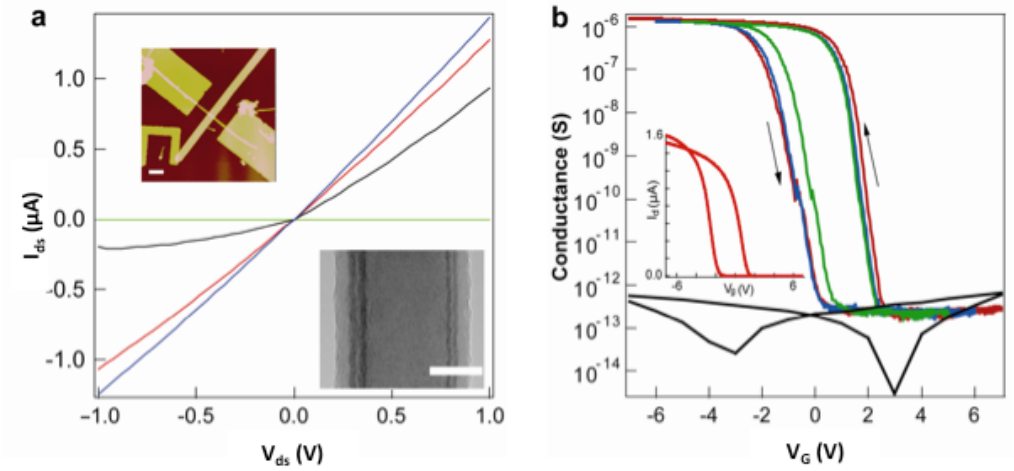
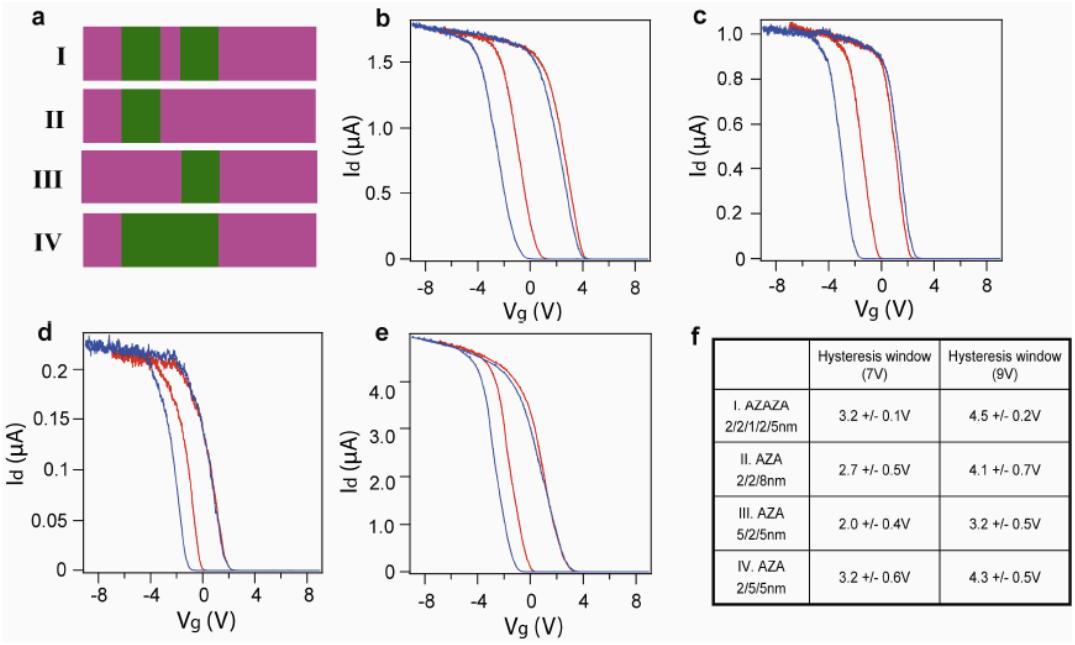


Figure 2-8 Electrical performance of CTNWFET. (a), I_{ds} – V_{ds} curves at -2V (blue), 0V (red), 2V (black), 6V (green) V_G. Upper left inset: AFM image of CTNWFET device. Scale bar: 1 μm. Lower right inset: TEM image of p-type Si/SiO2- ZrO_2-Al_2O_3-ZrO_2-Al_2O_3 core/shell nanowire. Note that TEM image reveals a well-defined interface between dielectric thin films. Scale bar: 20 nm. (b), Conductance vs. V_G curves with ±5V (green), ±6V (blue), and ±7V (red) V_G scanning ranges by a log-linear plot. Arrows indicate the direction of V_G scan. The black line corresponds to top-gate leakage current with ±7 V V_G scanning ranges, which is less than 1 pA. Inset: I_{ds}-V_G curve at 1 V V_{ds} by a linear plot.

Investigation of various multi-dielectric shell structures

In principle, charge trapping based on the band structure of a quantum well composed of tunneling, charge-trapping, and blocking layer, works. In order to investigate simpler but more functional structures, various combinations of multi-dielectric shell structure with varying thickness, order, and total number of dielectrics are tested. Fig. 2-9a shows conditions investigated, where total thickness is fixed and thickness and positions of Al_2O_3 and ZrO_2 varied; Fig. 2-9b-e gives the results. Fig. 2-9f lists the hysteresis window width ΔV_{th} corresponding to the charge-trapping capability of each structure; for all structures total thickness and average dielectric constant are similar. When we consider logic and memory components for the CTNWFET, larger ΔV_{th} is desirable for wider operational voltage with two different states. For this purpose, structure IV, 2nm-5nm-5nm Al_2O_3-ZrO_2-Al_2O_3, appears the best-suited. Interestingly, structure III shows the smallest ΔV_{th}, which is probably due to the same thick thickness of its tunneling and blocking layers. Due to this symmetry, the blocking layer can play the role of tunneling layer for the top-gate so that the injected electrons from the top-gate eventually decrease the total number of stored holes in charge trapping layer. It is noteworthy that the ΔV_{th} of the 2-nm ZrO_2 layer in structure II is smaller than that of the 4- and 5-nm ZrO_2 layers of structure I and IV, which could result in lower charge storage capacity and prove the charge-trapping functionality of the ZrO_2 layer. Based on this test, structure IV 2nm-5nm-5nm Al_2O_3-ZrO_2-Al_2O_3 (AZA) will be used as the gate oxide of CTNWFET in our multi-functional non-volatile crossbar arrays.



	Hysteresis window (7V)	Hysteresis window (9V)
I. AZAZA 2/2/1/2/5nm	3.2 +/- 0.1V	4.5 +/- 0.2V
II. AZA 2/2/8nm	2.7 +/- 0.5V	4.1 +/- 0.7V
III. AZA 5/2/5nm	2.0 +/- 0.4V	3.2 +/- 0.5V
IV. AZA 2/5/5nm	3.2 +/- 0.6V	4.3 +/- 0.5V

Figure 2-9 Investigation of CTNWFET performance with four different multi-dielectric shell structures. (a), Schematic of four different gate stacks with combinations of Al_2O_3 (purple) and ZrO_2 (green) layers. The detailed thickness is listed in (f). Note that the leftmost AlO_2 corresponds to the tunneling layer, and the rightmost AlO_2 could be the blocking layer. (b-e), $I_{ds} - V_G$ curves with ±7V (red) and ±9V (blue) V_G scanning ranges for structure I (b), II (c), III (d), and IV (e). (f), Table of composition, thickness, and hysteresis window width for the four structures.

2.5 Conclusion

In this chapter the design, fabrication, and characterization of core/shell NWFET with charge-trapping functionality was discussed. First, designed p-type Si/Al_2O_3-ZrO_2-Al_2O_3-ZrO_2-Al_2O_3 30nm/1nm-2nm-1nm-2nm-5nm core/shell NWFET was simulated and showed an

expected shift of threshold voltage due to the charge trapping originating from the quantum well of the shell structure. Next, specific details of the fabrication of general core/shell NWFET devices were provided. Finally, the designed CTNWFET was fabricated and characterized. The device demonstrated non-volatile bi-stable field-effect transistor device with high performance as predicted by theory. Furthermore, the investigation of various multi-dielectric shell structures for CTNWFET revealed a simple and more highly functional platform for logic and memory components. This CTNWFET will be a basic component of the more complex structures and circuits discussed in the next chapter.

Bibliography

1 *International Technology Roadmap for Semiconductors*, www.itrs.net

2 Tian, B., Zheng, X., Kempa, T. J., Fang, Y., Yu, N., Yu, G., Huang, J. & Lieber, C. M. Coaxial silicon nanowires as solar cells and nanoelectronic power sources. *Nature* **449**, 885-890 (2007).

3 Dong, Y., Yu, G., McAlpine, M. C., Lu, W. & Lieber, C. M. Si/a-Si core/shell Nanowires as nonvolatile crossbar switches. *Nano Lett*. **8**, 386-391 (2008).

4 Kempa, T. J., Tian, B., Kim, D. R., Hu, J., Zheng, X. & Lieber, C. M. Single and tandem axial p-i-n nanowire photovoltaic devices. *Nano Lett.* **8**, 3456-3460 (2008).

5 Lee, S., Jung, Y., & Agarwal, R. Highly scalable non-volatile and ultra-low-power phase-change nanowire memory. *Nature Nanotechnol.* **2**, 626-630 (2007).

6 Xiang, J., Lu, W., Hu, Y., Wu, Y., Yan, H. & Lieber, C. M. Ge/Si nanowire heterostructures as high-performance field-effect transistors. *Nature* **441**, 489-493 (2006).

7 Jiang, X., Xiong, Q., Nam, S., Qian, F., Li, Y. & Lieber, C. M. InAs/InP radial nanowire heterostructures as high electron mobility devices. *Nano Lett*. **7**, 3814-3218 (2007).

8 Solter, D. & McGrath, J. Completion of mouse embryogenesis requires both the maternal and paternal genomes. *Cell* **37**, 179-183 (1984).

9 Temple, S. The development of neural stem cells. *Nature* **414**, 112-117 (2001).

10 Rueckes, T., Kim, K., Joselevich, E., Tseng, G. Y., Cheung, C. & Lieber, C. M. Carbon nanotube-based nonvolatile random access memory for molecular computing. *Science* **7**, 94-97 (2000).

11 Bachtold, A., Hadley, P., Nakanishi, T. & Dekker, C. Logic circuits with carbon nanotube transistors. *Science* **9**, 1317-1320 (2001).

12 Duan, X., Huang, Y., Cui, Y. & Lieber, C. M. Nonvolatile memory and programmable logic from molecule-gated nanowires. *Nano Lett.* **2**, 487-490 (2002).

13 Huang, Y., Duan, X., Cui, Y., Lauhon, L., Kim, K. & Lieber, C. M. Logic gates and computation from assembled nanowire building blocks. *Science* **294**, 1313-1317 (2001).

14 Cui, Y. & Lieber, C. M. Functional nanoscale electronic devices assembled using silicon nanowire building blocks. *Science* **291**, 851-853 (2001).

15 Zhong, Z., Wang, D., Cui, Y., Bockrath, M. W. & Lieber, C. M. Nanowire crossbar arrays as address decoders for integrated nanosystems. *Science* **302**, 1377-1379 (2003).

16 Friedman, R. S., McAlpine, M. C., Ricketts, D. S., Ham, D. & Lieber, C. M. High-speed integrated nanowire circuits. *Nature* **434**, 1085 (2005).

17 Nam, S., Jiang, X., Xiong, Q., Ham, D. & Lieber, C. M. Vertically integrated, three-dimensional complementary metal-oxide-semiconductor circuits. *Proc. Natl. Acad. Sci. USA*, **106**, 21035-21038 (2009).

18 Hu, J., Ouyang, M., Yang, P., & Lieber, C. M. Controlled growth and electrical properties of heterojunctions of carbon nanotubes and silicon nanowires. *Nature* **399**, 48-51 (1999).

19 Cui, Y., Lauhon, L. J., Gudiksen, M. S., Wang, J. & Lieber, C. M. Diameter-controlled synthesis of single-crystal silicon nanowires. *Appl. Phys. Lett.* **78**, 2214-2216 (2001).

20 Wu, Y., Cui, Y., Huynh, L., Barrelet, C. J., Bell, D. C. & Lieber, C. M. Controlled growth and structures of molecular-scale silicon nanowires. *Nano Lett.* **4**, 433-436 (2004).

21 Park, W. I., Zheng, G., Jiang, X., Tian, B. & Lieber, C. M. Controlled synthesis of millimeter-long silicon nanowires with uniform electronic properties. *Nano Lett.* 8, 3004-3009 (2008).

22 McAlpine, M. C., Friedman, R. S., Jin, S., Lin, K., Wang, W. U. & Lieber, C. M. High-performance nanowire electronics and photonics on glass and plastic substrates. *Nano Lett.* **3**, 1531-1535 (2003).

23 Cui, Y., Zhong, Z., Wang, D., Wang, W. U. & Lieber, C. M. High performance silicon nanowire field effect transistors. *Nano Lett.* **3**, 149-152 (2003).

24 Sheriff, B. A., Wang, D., Heath, J. R & Kurtin, J. N. Complementary symmetry nanowire logic circuits: Experimental demonstrations and in silico optimizations. *ACS Nano* **2**, 1789-1798 (2008).

25 Dehon, A. Nanowire-based programmable architectures. *Acm. J. Emerg. Technol.* **1**, 109-162 (2005).

26 Scott, J. F. & Paz de Araujo, C. A. Ferroelectric memories. *Science* **15**, 1400-1405 (1989).

27 Tang, J., Wang, C., Hung, M., Jiang, X., Chang, L., He, L, Liu, P., Yang, H., Tuan, H., Chen, L. & Wang, K. L. Ferromagnetic germanide in Ge nanowire transistors for spintronics application. *ACS Nano.* **6**, 5710-5717 (2012).

28 Daughton, J. M. Magnetoresistive memory technology. *Thin Solid Films* **216**, 162-168 (1992).

29 Virk, H. S. & Kleemann, W. Multiferroic Memory: A disruptive technology or future technology? *Sol. St. Phen.* **189**, 1-14 (2012).

30 Nakayama, K., Kitagawa, T., Ohmura, M. & Suzuki, M. Nonvolatile memory based on phase transition in chalcogenide thin film. *Jpn. J. Appl. Phys.* **32**, 564-569 (1993).

31 Lee, S., Ko, D., Jung, Y., Agarwal, R. Size-dependent phase transition memory switching behavior and low writing currents in GeTe nanowires. *Appl. Phys. Lett.* **89**, 223116 (2006).

32 Lee, C., Hur, S., Shin, Y., Choi, J., Park, D. & Kim, K. Charge-trapping device structure of SiO_2/SiN/high-k dielectric Al_2O_3 for high-density flash memory. *Appl. Phys. Lett.* **86**, 152908 (2005).

33 Robertson, J. Band offsets of wide-band-gap oxides and implications for future electronic devices. *J. Vac. Sci. Technol. B* **18**, 1785-1791 (2000).

34 Sze, S. M. *Semiconductor Device – Physics and Technology* (John Wiley & Sons, 2002).

35 Fowler, R. H., Nordheim, L. Electron emission in intense electric fields. Proc. R. Soc. Lond. A 119, 173-181 (1928).

36 Gao, P. X., Song, J., Liu, J. & Wang, Z. L. Nanowire piezoelectric nanogenerators on plastic substrates as flexible power sources for nanodevices. *Adv. Mater.* **3**, 1531-1535 (2003).

37 *PMMA Positive Resists*, www.microchem.com

38 Zeghbroeck, B. V. *Principles of Semiconductor Devices and Heterojunctions* (Prentice Hall, 2009).

39 *Etchants*, www.transene.com

Chapter 3

Fully integrated configurable multi-functional CTNWFET crossbar array circuit

A computer processor constructed from intrinsically nanoscale building blocks and integrated on the nanoscale is a longstanding yet elusive goal of nanotechnology.[1-3] The important steps towards this goal over the last two decades include the demonstration of simple logic gates with assembled individual semiconductor nanowires and carbon nanotubes,[3-8] but with only 16 devices or less and a single function for each circuit. Small logic circuits also have been shown using a few elements of a 1D memristor array,[9] although these are passive devices without gain and thus difficult to cascade. These past circuits fall far short of a scalable, multifunctional nanoprocessor[10,11] due to challenges in materials, assembly, and architecture on the nanoscale. In this chapter, I will discuss the design, fabrication, and demonstration of the first programmable nanoprocessor system which surmounts these hurdles.

3.1 Physical design of CTNWFET crossbar array for programmable multi-functional complex circuit

Rational design of crossbar array architecture is an essential precursor to high-density complex circuitry with 1D building blocks because this rational design enables universal logic and signal restoration at the nanoscale. Fascinatingly, the combination of NW crossbar architectures with CTNWFET building blocks promises unique opportunities to realize high-density, complex circuits with programmable function.

First of all, one node out of the crossbar array can be considered from CTNWFET with a top-gate, as in Fig. 3-1a. The typical gate response of a p-type CTNWFET has a counterclockwise hysteresis curve, as shown Fig. 3-1b. Significantly, the $I_{ds} - V_G$ curve demonstrates that two distinct states are observed. After -6 V gate bias, the current I_{ds} of the device exhibited $>10^3$ nA change for V_G between -0.5 and 2.5 V, while in contrast, after +6 V gate bias, the current change was less than 20% for the same V_G range. We thus define the former state as 'active' since the CTNWFET behaves like an active transistor, while the latter state is 'inactive' since the device behaves as a passive interconnection. The programmability of individual NWFETs between the active and inactive states allows distinct functional circuits to be realized from arrays.

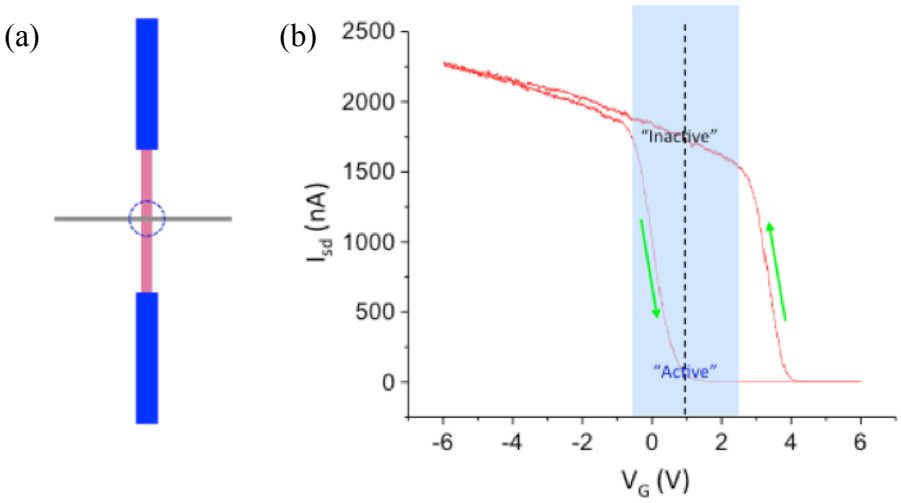


Figure 3.1

Figure 3.1 (Continued)

Figure 3-1 Structure and basic operation of one node based on the programmable CTNWFET. (a), A scheme of one node (blue dashed circle) generated by CTNWFET with a top-gate. The node is composed of source/drain (blue), charge-trapping functional NWFET (pink), and a top-gate on the NWFET (gray) (b), Typical I_{sd}-V_G curve of the node. "Active" and "inactive" states can be defined between -0.5V and 2.5V of V_G (light blue region).

Based on our understanding of the 1 x 1 case (Fig. 3-1a), the logic gates of an n x 1 nanowire crossbar array (NW-CA) consisting of n metal nanowires and one CTNWFET can be predicted after programming nodes. For example, Fig. 3-2 shows two schemes of 1 x 4 arrays where the resistor R is connected to both the drain and source. The main point of these circuits is that the connection between CTNWFET and the resistor R can be described as a simple voltage divider circuit as shown in Fig. 3-2. If the resistor connects to the source (Fig. 3-2a) and the resistance of CTNWFET, which is modulated by the top-gates, has much larger impedance than R, the output will be V_{ds} which can be defined as '1' state. In the opposite instance, the output will be 0 V which can be defined as '0' state. Hence, by programming the resistance modulation of the device, the inputs at active nodes on CTNWFET are included in logic flow so that the final output becomes a NOR gate of all inputs from only active nodes. For example, programming the nodes to active states for 'A' and 'B' and inactive states for 'C' and 'D' as in Fig. 3-2a will enable the circuits to operate an A NOR B circuit. More fascinatingly, the operation of logic gates can be changed by reprogramming the nodes so that fifteen different NOR logic combinations can be realized in one circuit feature as listed in Table 3-1. If the resistor is

connected to the drain (Fig. 3-2b), the circuit performs OR logic operations with active nodes after programming by the same mechanism as the NOR case.

Table 3-1 Possible logic gates of a 4 ×1 CTNWFET crossbar array of Fig. 3-2a by the node programming

Node state for input A	Node state for iput B	Node state for input C	Node state for input D	Logic operation
Active	Inactive	Inactive	Inactive	A
Inactive	Active	Inactive	Inactive	B
Inactive	Inactive	Active	Inactive	C
Inactive	Inactive	Inactive	Active	D
Active	Active	Inactive	Inactive	A NOR B
Active	Inactive	Active	Inactive	A NOR C
Active	Inactive	Inactive	Active	A NOR D
Inactive	Active	Active	Inactive	B NOR C
Inactive	Active	Inactive	Active	B NOR D
Inactive	Inactive	Active	Active	C NOR D
Active	Active	Active	Inactive	A NOR B NOR C
Active	Inactive	Active	Active	A NOR C NOR D
Inactive	Active	Active	Active	B NOR C NOR D
Active	Active	Inactive	Active	A NOR B NOR D
Active	Active	Active	Active	A NOR B NOR C NOR D

This concept can be expanded up to an n x n NW-CA as well as ‘even tiles’ of n x n NW-CAs, which are composed of n metal nanowires on n CTNWFETs. Fig 3-2c shows one example of a (4 x 3) x (3 x 1) NWCA which demonstrates ‘(B NOR D) NOR (A NOR B NOR D) NOR (A NOR D)’ logic gates after node programming as shown in Fig. 3-2c. The significant advantage of this strategy is that any kind of logic gates can be achieved by using tiles of

CTNWFET crossbar arrays, because the NOR gate is one of the universal gates.[13] Fig. 3-2d represents full-adder logic constructed with two blocks of CTNWFET crossbar arrays giving NOR combinations through node programming.

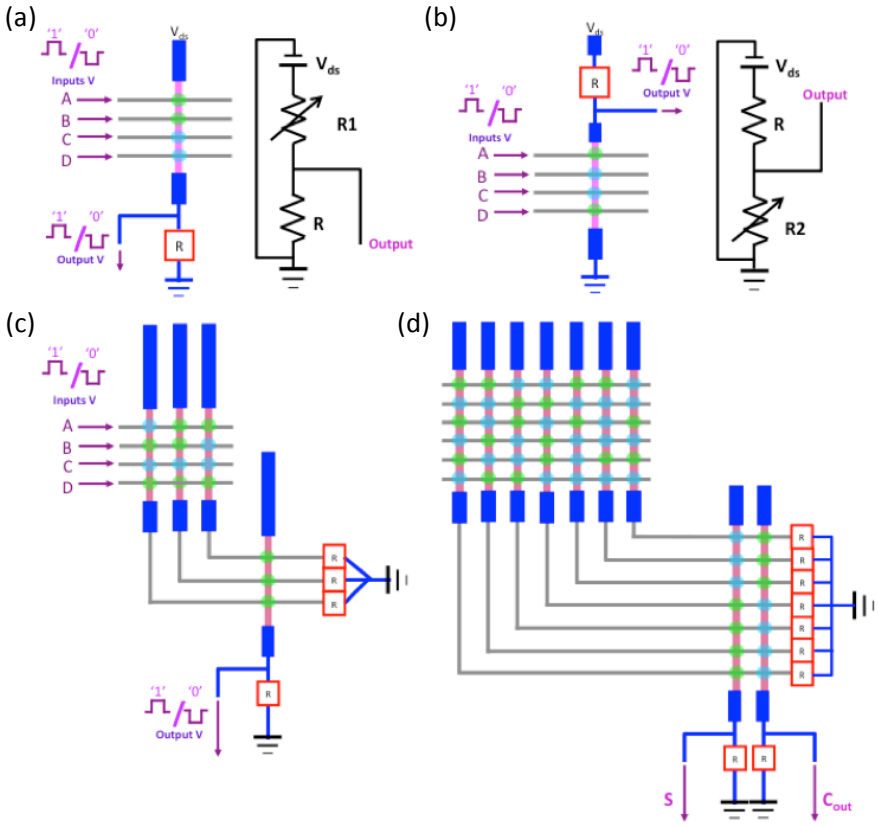


Figure 3-2 Schemes of n ×n CTNWFET crossbar array (CTNWFET-CA) for NOR or OR logics gates. A green dot and a blue dot correspond to active and inactive states programmed by a short pulse of large top-gate bias. R represents a load resistance which has similar value to the NWFET resistance. (a), 4 ×1 CTNWFET-CA for A NOR B logic operation. Note that the load resistor R is connected to source. At the left is the equivalent circuit. (b), 4 ×1 CTNWFET-CA for A OR D logic operation. Note that the load resistor R is connected to drain. The left shows the equivalent circuit. (c), (4×3)×(3×1) CTNWFET-CA for (B NOR D) NOR (A NOR B NOR D) NOR (A NOR D). (d), Full-adder circuit configuration by CTNWFET-CA.

Furthermore, tiles of n x n CTNWFET-CA are cascaded by feeding the outputs of one tile to the inputs of the next tile, forming a feed-forward logic architecture capable of combinational logic functions (Fig. 3-3). Sequential logic functions such as latches can be implemented by integrating control gates[14] or switchable diodes[15] in the architecture to allow for feedback, and eventually, this architecture leads to the realization of a nanoprocessor capable of logic, encoding/decoding, and memory functions. Here I will discuss the realization of these CTNWFET-CA architectures and demonstrate programmable multi-functional complex circuits for a nanoprocessor.

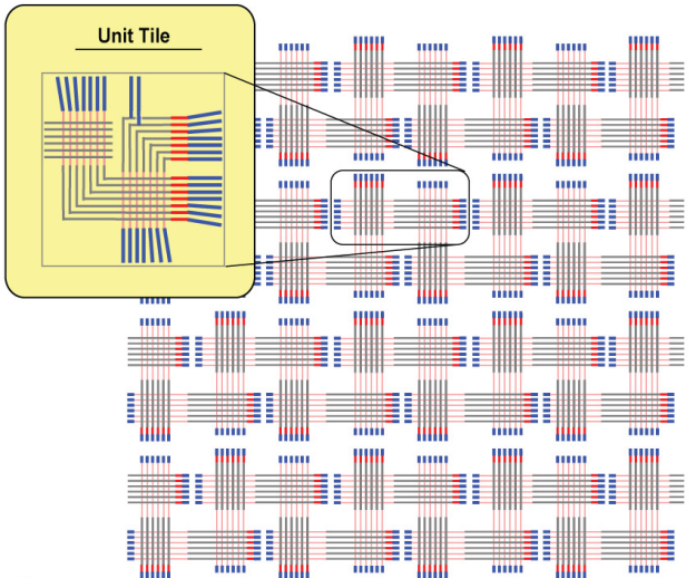


Figure 3-3 Nanoprocessor architecture based on the CTNWFET logic tile. The unit tile (dashed box) corresponds to two CTNWFET-CAs, block-1 (left) and block-2 (right). Each block contains charge-trapping NWs (pink), metal gate electrodes (gray), passive load resistances (red) and lithographic-scale electrodes (blue) integrated for input/output. Note that the CTNWs and metal gates in block-1 are rotated 90^{o} with respect to the schematic shown in 'Unit tile'.

3.2 Development of novel CTNWFET toward uniform performance

As discussed previously, a fundamental requirement for a basic building block in electronics is uniform performance across individual devices. In particular, the fluctuation of device performance is extremely critical for complex circuits such as a processor, where large quantities of devices must be coupled to each other and operated organically[16]. This requirement holds also for electronic circuits based on CTNWFET crossbar array. Specifically, the deviation of V_{th} in both active and inactive states must be smaller than the V_{th} separation between the two states. However, CTNWFETs based on p-type Si cores demonstrate several-volt fluctuations of V_{th} in both active and inactive states as shown in Fig. 3-4. Therefore, we use intrinsic Ge (Ge)/intrinsic Si (Si) core/shell nanowires for the semiconducting channel of the CTNWFET to address this critical issue, because the Ge/Si nanowire FET has shown not only exceptional electrical performance but also uniformity through bandgap engineering. The single-component semiconducting NWFET typically has Schottky barriers at metal contacts and low intrinsic mobility from scattering from charged dopants which significantly limit device performance and uniformity, while Ge/Si nanowire FET shows transparent contacts and low-bias ballistic transport from one-dimensional hole gas system through 1D subbands, enabling high performance and uniformity.[17-19]

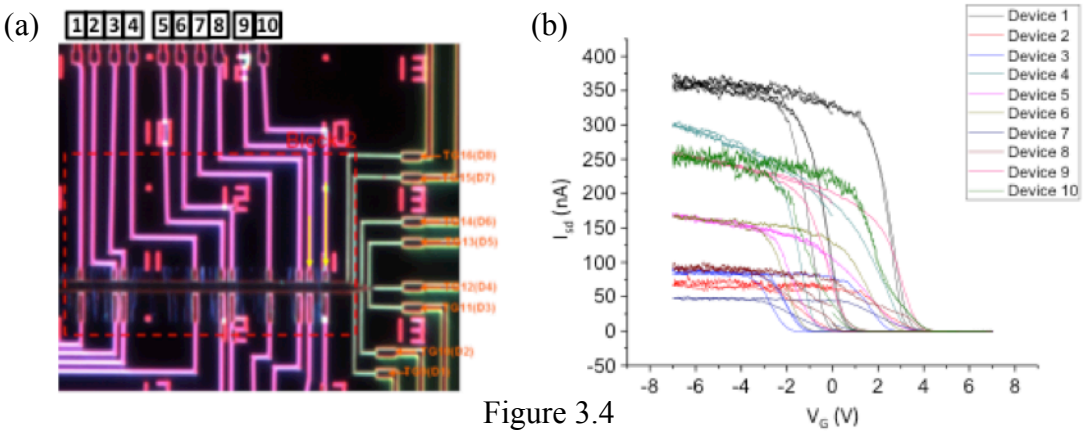


Figure 3.4

Figure 3.4 (Continued)

Figure 3-4 Non-uniform performance of Si-based CTNWFETs. (a), Dark-field optical microscope image of a 8 ×10 Si-based CTNWFET-CA block. (b), Ids vs. VG curves of ten Si-based CTNWFETs in the block of (a). The device number corresponds to the number in (a). Note that individual devices show different on-current, threshold voltage of active/inactive state, and hysteresis window width.

Fig. 3-5b and c demonstrate outstanding uniform performance of (Ge/Si)/Al_2O_3-ZrO_2-Al_2O_3 (AZA) core/shells in block-1 and block-2 of the CTNWFET crossbar arrays (CTNWFET-CA) (Fig. 3-5a) of which fabrication will be discussed in the next section. Fig. 3-5b shows the typical I_{ds}-V_G curves of Ge/Si CTNWFETs in block-1 (left array in Fig. 3-5a) and block-2 (right array in Fig. 3-5a), in which the performances of eight top-gates almost overlap with each other. Specifically, the deviation of V_{th} in both active and inactive states must be smaller than the V_{th} separation between the two states. The V_{th} of 70 CTNWFET nodes from block-1 of the CTNWFET-CA structure in both active and inactive states was characterized (Fig. 3-5c). Notably, 59 out of 70 (84%) of nodes in the active state had V_{th}'s < 2V and 64 out of 70 (91%) of those in the inactive state had V_{th}'s >3.5 V (Fig. 3-5c, lower and upper planes, respectively). The high yield of NWFET devices reflects the uniformity of the Ge/Si CTNWFET building block,[13] while controlled assembly[20] allows any defective elements to be excluded readily from the functional circuit. We thus readily achieve a distinction between V_{th}'s for both states in both blocks of the CTNWFET-CA, which provide a relatively wide ~2V hysteresis window for circuit operation. Therefore, these Ge/Si CTNWFET-CA tiles are the best candidates for

implementation as the unit of novel programmable multi-functional complex circuit, as will be demonstrated in later sections.

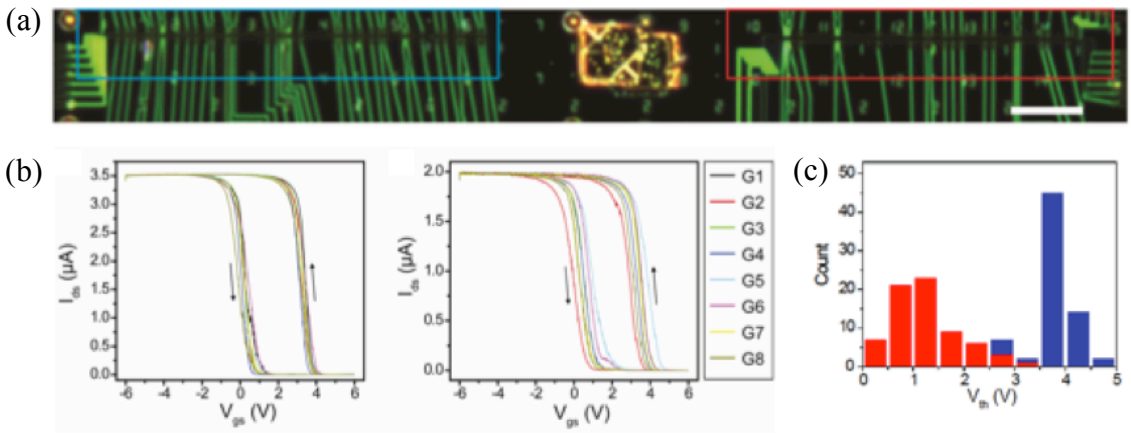


Figure 3-5 Uniform performance of Ge/Si-based CTNWFET. (a), Dark-field optical microscope image of the two-block CTNWFET-CAs. The cyan (left) and red (right) open rectangles outline block-1 and block-2, respectively. Scale bar: 40 μm. (b), Typical I_{ds} vs. V_{gs} data of Ge/Si-based CTNWFET devices in block-1 (left curves, cyan box in (a)) and block-2 (right curves, red box in (b)). The devices are biased at 0.5 V. The measurement is taken by scanning the V_{gs} on one gate line from 6 V to -6 V and then back to 6 V, while keeping the other gate voltages at 0 V. Prior to the measurement all the gate lines are biased at 6 V for 5 s to reset all of the CTNWFET nodes into inactive state. The arrows mark the direction of the hysteresis. The different colored curves represent recording from different gate lines (G1 ~ G8). (c), Distribution of V_{th} from 70 NWFET nodes in block-1 (cyan box in (a)) in the CTNWFET-CA tile. The blue and red bars represent the V_{th} values of devices in inactive and active states, respectively, with V_{ds} = 0.5 V

3.3 Fabrication of CTNWFET crossbar arrays for circuitry

The development of effective assembly is a prerequisite to building highly integrated functional nanosystems with nanowire building blocks. In particular, the hierarchical organization of CTNWFET at high density on a large scale is a critical precursor to the fabrication of a nanoprocessor.[21] Since the 21st century, several methods have been developed to align nanowires axially on the substrate, including electric field,[22, 23] microfluidic flow,[24] Langmuir-Blodgett film,[25, 26] blown-bubble films[27] and contact printing.[20, 28] Herein, I describe the lubricant-assisted contact printing method which is one of the simplest methods of fabricating density-controllable NW arrays on a large scale to be used for CTNWFET-CAs.

Ge/Si NWs are transferred from growth substrates to device substrates by a shear printing process where shear force determines the density and alignment of NWs.[28] First, oxygen plasma treated (100 W, 1 min) device substrates (600 nm SiO_2/Si) are patterned by photolithography (Shipley S1805 diluted by 50 % in Thinner-P, MicroChem) to define a region where NWs will be deposited. The dimension of the region is typically ~1 cm (width) by ~0.1 cm (length). Second, the patterned device substrate is mounted onto a fixed stage whose movement is controlled by a micromanipulator. Approximately 50 μL of heavy mineral oil (Sigma-Aldrich) is drop-casted onto the device substrate to serve as a lubricant. Third, the NW growth substrate (~1 cm by ~2 cm) is brought into contact with the device substrate (NWs facing the device substrate) and a pressure of ~3.4 N/cm^2 is applied while the device substrate is slid with a constant velocity of ~5 mm/min (Fig. 3-6a). These procedures produced an average printing density of ~2 Ge/Si NW per micron as shown in Fig. 3-6b.

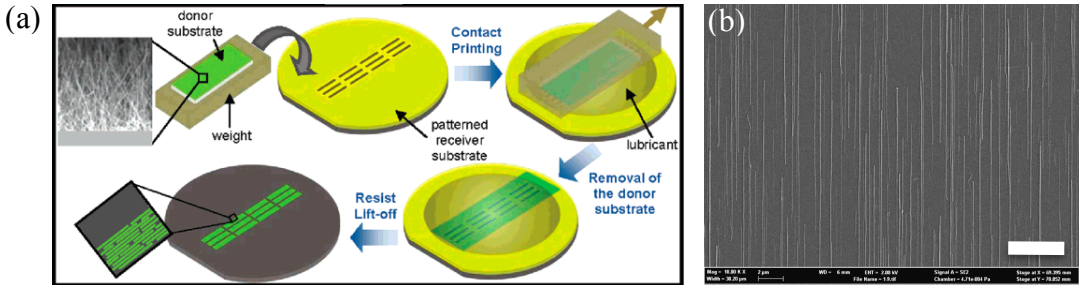


Figure 3-6 Procedure and result of lubricant-assisted contact printing method for Ge/Si NWs. (a), Schematic of process flow contact printing. (b), Axially aligned Ge/Si NWs with ~2 NWs per micron density on 600 nm SiO_2/Si substrate after all contact printing processes completed. Scale bar: 4 μm

The large-area Ge/Si NW array is first patterned into proper dimensions for device fabrication, using an inductively coupled plasma reactive ion etching (ICP-RIE, Surface Technology Systems). SF_6 is used as etchant and electron beam lithography (EBL, with PMMA 950-C2, Microchem) is used to mask regions for devices. Dark-field optical microscopy is used to register the positions of individual Ge/Si NWs, and then source/drain contacts are defined by EBL followed by wet etching in 1:7 buffered oxide etchant (BOE, Transene) for 5 seconds and thermal evaporation of 70 nm Ni. The dielectric layers are deposited by ALD followed by EBL and metallization to define top-gate metal lines (Cr/Au, 1.5/70 nm respectively). The dielectric over the outer metal is etched with 1:7 BOE for 20 s to allow electrical access to the devices. Finally, EBL and metal evaporation were used to connect source/drain/gate electrodes to the outer metal pads.

Fig. 3-5a and 3-7b show optical microscope images and SEM images of a unit tile composed of two CTNWFET-CA blocks which have undergone all fabrication steps as shown schematically in Fig. 3-7a. A total of 496 programmable NWFET devices were laid out in two separate arrays with a total area of approximately 960 μm^2, where each device node consists of a single CTNW crossed by a top-gate line. The average area per node, ~1.9 μm^2, is relatively large in these proof-of-concept studies but does not represent a lower limit, as previous studies demonstrating close-packed NW assembly[26] and the scaling of charge-trapping devices[29] indicate that an area a thousand times smaller, ~0.0017 μm^2, is achievable.

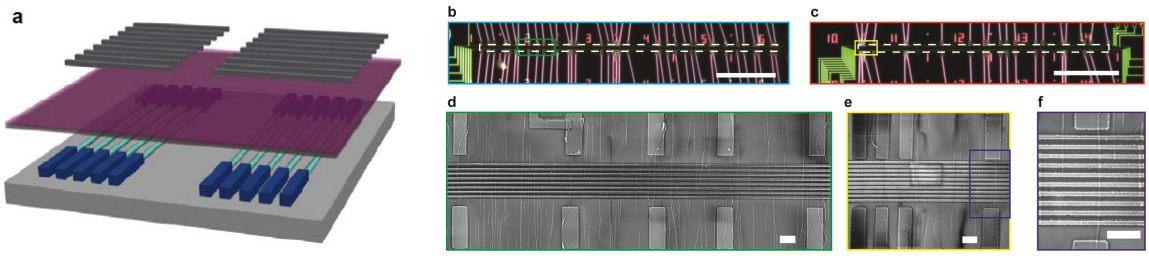


Figure 3-7 Fabrication and structure of CTNWFET-CA tile. (a), Conceptual illustration of key components of the two-block CTNWFET tile, including assembled and patterned Ge/Si NWs (cyan) with source/drain electrodes (blue), charge-trapping tri-layer gate dielectric (purple) and metal top-gate lines (gray). The fabricated structure consists of two blocks of CTNWFETs, namely block-1 (left) and block-2 (right). (b-c), Dark-field optical image of the block-1 and the block-2 from the region defined by the cyan rectangle and the red rectangle in Fig. 3-5a. The white dashed box at the central region of the image outlines the region containing NWFET devices. Scale bar: 40 μm. The total area of the regions defined by the white dashed boxes in b and c is ~960 μm^2. Scale bar: 40 μm. (d), SEM image of the region defined by the green rectangle in (b). Scale bar: 1 μm. (e), SEM image of the region defined

Figure 3-7 (Continued) by the yellow rectangle in (c). Scale bar: 1 μm. (f), SEM image of the region defined by the blue rectangle in (e), showing a single-NW device with 10 top-gates. Scale bar: 1 μm. The optical images are taken under in the dark-field mode (BX51, Olympus) with 20× (b,c) objective lenses. SEM images were taken in a field-emission SEM (Ultra55, Zeiss) with 2 kV acceleration voltage and in-lens detector.

3.4 Demonstration of fully integrated programmable multi-functional complex circuit based on CTNWFET-CAs

As discussed in section 3.1, the two-block CTNWFET-CA tile can be programmed for various Boolean functions. Theoretically, the same tile can demonstrate a range of distinct logic operations since active and inactive nodes in both blocks are reproducibly and independently switched by voltage programming. Therefore, based on a multi-channel measurement system capable of applying node programming (see appendix B for detailed information), I will demonstrate a fully integrated programmable multi-functional complex circuit fabricated for the first time via a bottom-up approach. The important combinational circuits, which play a fundamental role in the nanoprocessor, such as full-adder, full-subtractor, multiplexer and demultiplexer, will be exemplified on the same CTNWFET-CA tile through electrical reconfiguration of nodes.

Demonstration of a full-adder

Fig. 3-8a illustrates the configuration of the 1-bit full-adder logic circuit comprising two blocks with the output of block-1 (left dashed box, Fig. 3-8a) fed to the input of block-2 (right

dashed box, Fig. 3-8b). The programmed active (green dots, Fig. 3-8a) and inactive nodes determine the circuit function, and for this full-adder case the outputs S and C_{out} represent the sum and carry-out of the summation ($A + B + C$), respectively, with $S = A \oplus B \oplus C$ and $C_{out} = (A \cdot B) + (A \cdot C) + (B \cdot C)$. The symbols '$\oplus$', '$\cdot$' and '+' represent logical XOR, AND and OR, respectively. Six inputs A, $\overline{A}$ (NOT A), B, $\overline{B}$ (NOT B), C, and $\overline{C}$ (NOT C) based on 0V pulse for '0' state and 3 ~ 3.6V pulse for '1' state are applied to the unit tile and collected output S and C_{out}. In this demonstration, because V_{DD} in block-2 is 0.1 V, the full swing of output voltage of S and C_{out} is 0.1V which is not matched to input voltage. The input/output matching in the full-adder circuit will be discussed later. The data successfully show correct full-adder results corresponding to the full-adder truth table (Table 3-2) and setting half swing to 0.04V.

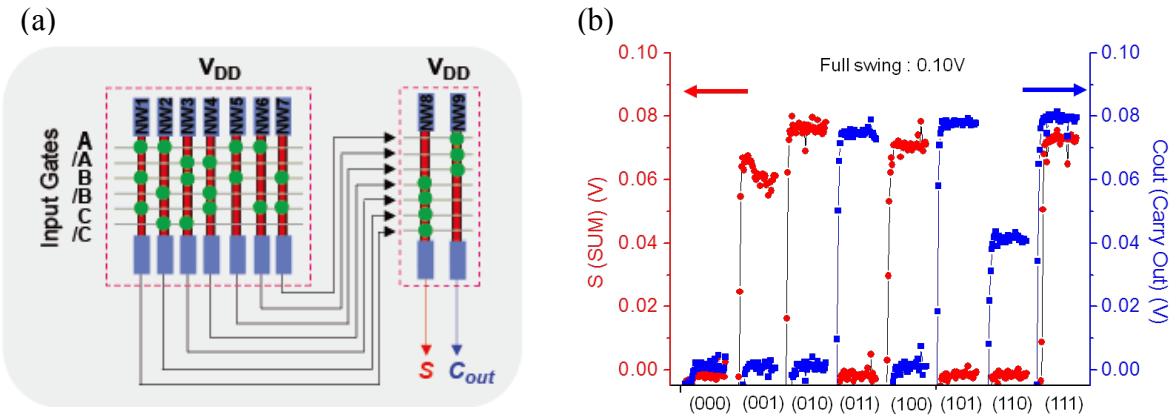


Figure 3-8 Demonstration of a full-adder circuit. (a), Circuit design implementing a 1-bit full-adder. /A, /B and /C denote the complementary inputs of A, B and C, respectively. The left and right dashed boxes outline block-1 and block-2 respectively. Applied V_{DD} in block-1 and V_{DD} in block-2 are 1.5V and 0.1V respectively. Load resistance connected to sources of each CTNWFET is omitted in schematic. (b), Output voltage levels for S and C_{out} at all possible eight input states.

Table 3-2 Truth table of full-adder logic and results of all eight input states in Fig. 3-8b

A	B	C_{in}	Theoretical expectation		Experimental results (Fig. 3-8b)	
			S	C_{out}	S	C_{out}
0	0	0	0	0	0 (0.000V)	0 (0.002V)
0	0	1	1	0	1 (0.065V)	0 (0.002V)
0	1	0	1	0	1 (0.077V)	0 (0.001V)
0	1	1	0	1	0 (0.000V)	1 (0.075V)
1	0	0	1	0	1 (0.071V)	0 (0.002V)
1	0	1	0	1	0 (0.000V)	1 (0.078V)
1	1	0	0	1	0 (0.000V)	1 (0.042V)
1	1	1	1	1	1 (0.072V)	1 (0.080V)

Demonstration of a full-subtractor

After reprogramming the same tile (Fig. 3-5a) as Fig. 3-9a, The two outputs of the reprogrammed circuit, D and B_{out}, represent the difference and borrow, respectively, of the subtraction (*X*-*Y*-*B*) with the logic relations $D = X \oplus Y \oplus B$ and $B_{out} = B \cdot \overline{(X \oplus Y)} + \overline{X} \cdot Y$, where *X*, *Y* and *B* are the inputs to the circuit and $\overline{X}$ represents the complementary input of *X*. Measurements of D and B_{out} for different *X*-*Y*-*B* input combinations (Fig. 3-9b) based on the same conditions in terms of input voltages and V_{DD} in block-1 and block-2 show that the output voltage levels for logic "0" (0 – 0.01 V) and logic "1" (0.04 – 0.08 V) are well separated and represent robust states. Moreover, the truth table summarizing the expected and experimental results for the full-subtractor (Table 3-3) demonstrates full and correct logic of this processing unit. This result explicitly shows that CTNWFET-CA tile can perform multi-functional complex logic operations with one physical feature.

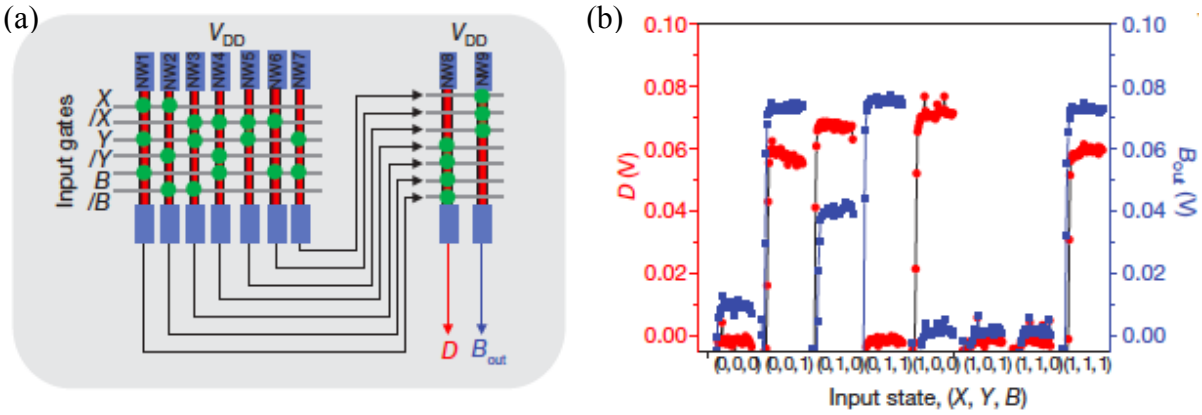


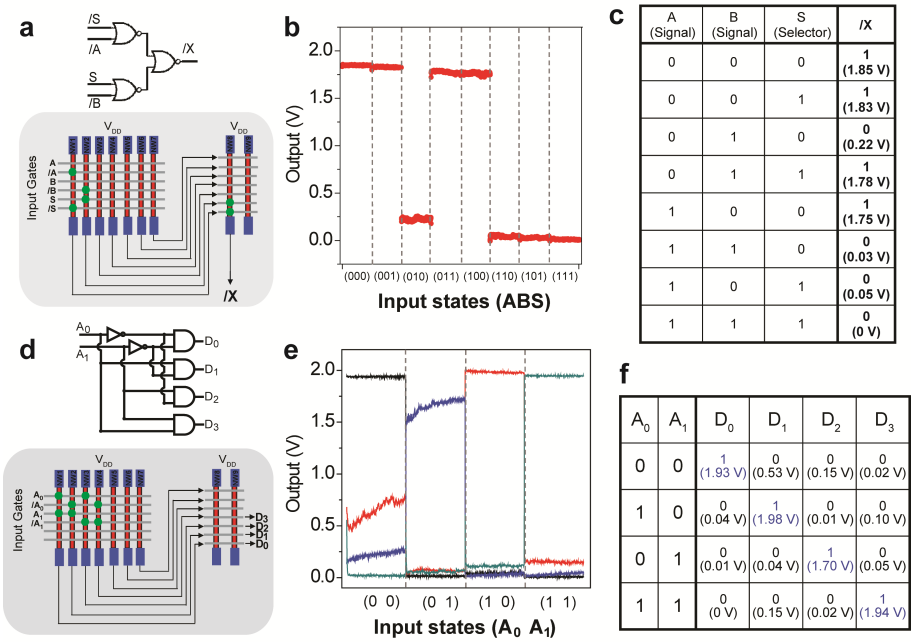
Figure 3-9 Demonstration of a full-subtractor circuit. (a), Schematic of a circuit implementing a full-subtractor. /X, /Y and /B denote the complementary inputs of X, Y and B, respectively. Applied V_{DD} in block-1 and V_{DD} in block-2 are 1.5V and 0.1V respectively. Load resistance connected to sources of each CTNWFET is omitted in schematic. (b), Output of D (red) and B_{out} (blue) of the full-subtractor implemented with the same tile structure shown in Fig. 3-5a with all eight input states.

Table 3-3 Truth table of full-subtractor logic and results of all eight input states in Fig. 3-9b

X	Y	B_{in}	Theoretical expectation		Experimental results (Fig. 3-9b)	
			D	B_{out}	D	B_{out}
0	0	0	0	0	0 (0.000V)	0 (0.009V)
0	0	1	1	1	1 (0.059V)	1 (0.072V)
0	1	0	1	1	1 (0.068V)	1 (0.040V)
0	1	1	0	1	0 (0.000V)	1 (0.076V)
1	0	0	1	0	1 (0.070V)	0 (0.002V)
1	0	1	0	0	0 (0.000V)	0 (0.002V)
1	1	0	0	0	0 (0.000V)	0 (0.002V)
1	1	1	1	1	1 (0.060V)	1 (0.074V)

Demonstration of multiplexer/demultiplexer

The multiplexer and demultiplexer can be expressed by combinations of the NOR universal gates as discussed in the section 3.1 so that the node configuration of the two-block CTNWFET-CA tile can be designed for a 2-to-1 multiplexer and 2-to-4 demultiplexer as in Fig. 3-10a and Fig. 3-10d respectively. For 2-to-1 multiplexer demonstration, two signals *A* and *B*, and one selector *S* based on 0V pulse for '0' state and 3 ~ 3.6V pulse for '1' state are input to the reprogrammed unit tile as Fig. 3-10a and multiplexed to the output $\overline{X}$ from the one CTNW in block-2 while applying 1.5V and 2.2V at V_{DD} in block-1 and block-2 respectively. The output $\overline{X}$ voltage levels for logic "0" (0 – 0.22 V) and logic "1" (1.75 – 1.85 V) are clearly defined in 1.0 V half swing (Fig. 3-10b and c). For the 2-to-4 demultiplexer demonstration, two signals A_0 and A_1 are demultiplexed to four outputs D_0, D_1, D_2, and D_3 from the reconfigured unit tile as shown in Fig. 3-10d with the same condition regarding inputs and V_{DD}s. The outputs show unambiguous voltage levels for logic "0" (0 – 0.53 V) and logic "1" (1.70 – 1.98 V) considering 1.0 V half swing voltage. (Fig. 3-10e and f)



A (Signal)	B (Signal)	S (Selector)	/X
0	0	0	1 (1.85 V)
0	0	1	1 (1.83 V)
0	1	0	0 (0.22 V)
0	1	1	1 (1.78 V)
1	0	0	1 (1.75 V)
1	1	0	0 (0.03 V)
1	0	1	0 (0.05 V)
1	1	1	0 (0 V)

A_0	A_1	D_0	D_1	D_2	D_3
0	0	1 (1.93 V)	0 (0.53 V)	0 (0.15 V)	0 (0.02 V)
1	0	0 (0.04 V)	1 (1.98 V)	0 (0.01 V)	0 (0.10 V)
0	1	0 (0.01 V)	0 (0.04 V)	1 (1.70 V)	0 (0.05 V)
1	1	0 (0 V)	0 (0.15 V)	0 (0.02 V)	1 (1.94 V)

Figure 3.10

Figure 3.10 (Continued)

Figure 3-10 Multiplexer and demultiplexer circuits implemented in CTNW logic tile architecture. (a-c), Characterization of a 2-to-1 multiplexer. (a), Schematic of logic (upper) and circuit implementation (lower) of multiplexer. The circuit involves 2 CTNWs in block-1, 1 CTNW in block-2 and 6 input gates (A, B, S, and complements). The S signal selects the output X between A and B. Note that in this demonstration the complementary signal (/X) is generated, which can be easily translated to X by using an additional NWFET as an inverter. (b), Voltage output (/X) at 8 input states. The circuit was realized using the same CTNWFET-CA tile structure shown in Fig. 3-5a. (c), Truth table of the multiplexer. The measured voltage outputs are summarized in the brackets. (d-f), Characterization of a 2-to-4 demultiplexer. (d), Schematic of logic (upper) and circuit implementation (lower) of the demultiplexer. The circuit uses 4 CTNWs in block-1 and 4 gates (A_0, A_1 and their complementary inputs). The 4 outputs ($D_0 – D_3$) are addressed by combinations of (A_0, A_1). (e), Voltage output of D_0 (black), D_1 (red), D_2 (blue) and D_3 (cyan) at different (A_0, A_1) input states. (f), Truth table of the demultiplexer. The measured voltage outputs are summarized in brackets. The blue color marks the line that is selected at each input combination.

Input/output matching for cascade configuration

To restore signals, expand the size of logic gates and cascade logic flows, conserving or amplifying the output relative to the input in the unit tile, namely input/output (I/O) voltage matching, is crucial. In this respect, FET-based logic gates have a huge advantage due to their larger-than-unity gain property,[30] unlike passive memristor devices[9] where the gain is <1.

Specifically, this I/O matching is a prerequisite for a complex circuit requiring self-feedbacks such as a latch and shift register that are sequential circuit elements in a processor. The I/O matching properties of two CTNWFET-CA tiles used for the full-adder, the full-subtractor, and multiplexer/demultiplexer will be explored with the full-adder configuration and implemented to Data latch[31] (D-latch) after reconfiguration.

Typical voltage transfer functions of the full-adder circuit (Fig. 3-8a) for power-supply voltage, V_{DD}, of 3.0V (Fig. 3-11a) show that as the input levels of *A*, *B* and *C* are swept from logic state "0" (0V) to logic state "1" (3.5V), the outputs S and C_{out} switch from logic "0" (both 0 V) to logic "1" (2.0 and 2.7V, respectively). From these data, the peak voltage gains of C_{out} and S (Fig. 3-11a, lines tangential to data) are found to be 10 and 4, respectively, which show the larger-than-unity gain and the matching of input–output voltage levels needed for a potential to cascade the logic tiles (Fig. 3-3). Further tests show that the output of S and C_{out} for six typical input combinations (Fig. 3-11b) all had similar output ranges: 0 – 0.6 V for logic state "0" and 2.0 – 2.7 V for logic state "1". The expected and experimental results for a full adder are summarized in a truth table (Fig. 3-11c), which shows good consistency for this fundamental logic unit. The V_{th} value of some active NWFET nodes shifted with the 3V source bias and precluded switching behavior for the (*A*, *B*, *C*) = (0, 1, 0) and (0, 1, 1) inputs for a consistent input voltage range (0 – 3.5 V). It is worthwhile to note that optimization of logic operations can be achieved by tuning V_{DD} and the load resistance, together with adjustment of V_{th} through the choice of top-gate metal[18]. Nonetheless, the large voltage gain and matching of input–output voltage levels described here demonstrates the potential to integrate the prototype device into large-scale integrated circuits such as a multi-bit adder in a cascade configuration.

Encouraged by the results of I/O matching, we mapped a D-latch, a sequential logic circuit capable of information storage, onto the unit tile (Fig. 3-11d). The D-latch circuit (Fig. 3-11d, upper panel) is composed of four NOR gates with a positive-feedback connection between the output, *Q*, and inputs to NOR gates 2 and 3 (Fig. 3-11d, upper panel). As a consequence, *Q* equals input data, *D*, when clock, *E*, is in logic state "1" but retains its previous value when *E* is switched into logic state "0". We implemented the NOR gates in the tile using NW1–NW3 in block 1 and NW8 in block-2 (Fig. 3-11d, lower panel), and formed the positive feedback by connecting the output to an input gate in block-1. An important constraint on realizing the D-latch logic is that there must be a successful feedback loop (output *Q* of block-2 back to block-1; Fig. 3-11d), which requires matching of input and output voltage levels. Measurement of *Q* as a function of repetitive *E* and *D* pulses (Fig. 3-11e) shows that *Q* follows *D* when *E* is switched to logic "1" (3.6 V) at time points 16 and 33 s but retains its previous value when *E* is switched to logic "0" (0 V) at 7, 24 and 41 s, as expected for a D-latch. The robustness of this sequential logic circuit is tested further by inputting a more complex data waveform (Fig. 3-11f), where measurements of *Q* demonstrated a sharp logic operation by following *D* with high fidelity in the time intervals 16 – 24 and 33 – 41 s. Moreover, the voltage range of output, *Q* (0 – 2.2 V), closely matches that of the input data, *D*, and clock, *E*. These data clearly show the successful operation of D-latch function in a programmable CTNWFET-CA tile based on I/O matching.

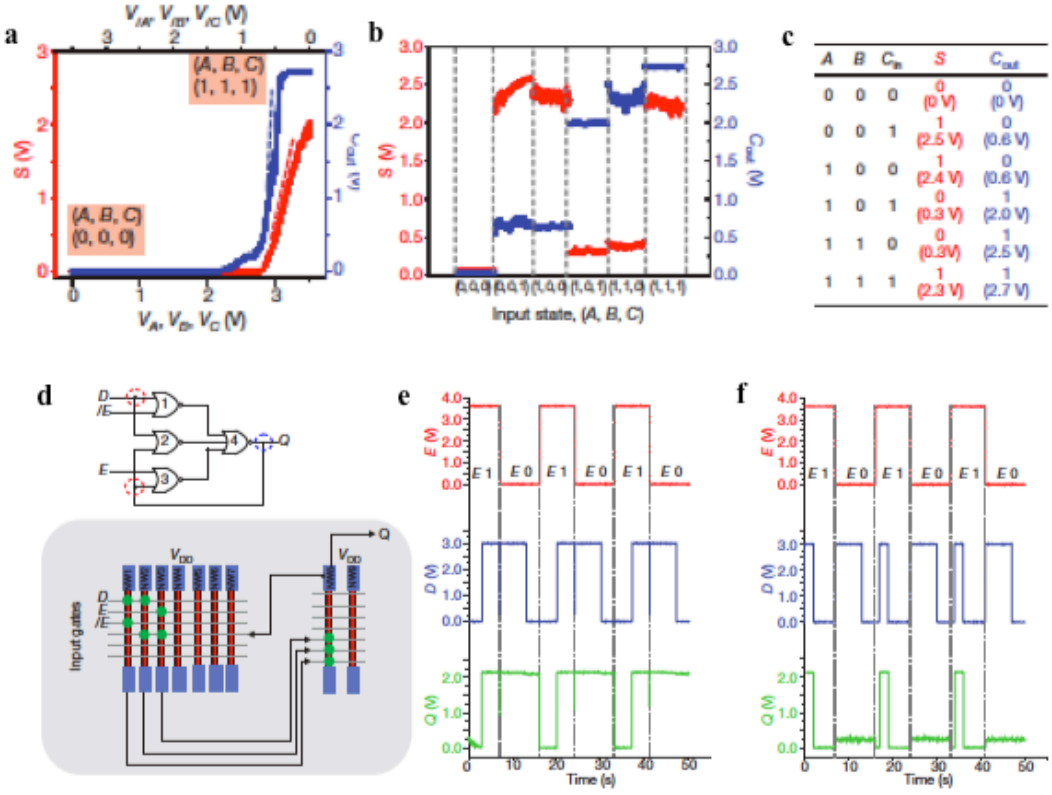


Figure 3-11 Demonstration of a full-adder and D-latch based on input/output matching. (a-c), Characterization of full-adder with I/O matching. (a), Voltage transfer function for S (red) and C_{out} (blue) from input states (0, 0, 0) to (1, 1, 1). The dashed tangent lines show the maximal voltage gains of the outputs. (b), Output voltage levels for S and C_{out} for six typical input states. (c), Truth table of full-adder logic for the six input states in (b). The measured output voltages are shown in brackets. (d-f), Demonstration of D-latch. (d), Schematics of logic (upper) and circuit design (lower) of a D-latch implemented with the same CTNWFET-CA tile used in (a–c). (e, f), Output,Q, waveforms (green) at two sets of clock (E, red) and data (D, blue) inputs.

3.5 Comparison between nanowire logic tiles and 32-nm state-of-the-art CMOS logic

The reversible programming of individual CTNWFET nodes in the tile provides great versatility, as shown by the combinational and sequential circuit elements demonstrated above. Reconfigurable logic has been realized using memristor complementary metal–oxide–semiconductor (CMOS) hybrid circuits[32], where the microscale CMOS layer is responsible for logic operation and memristors are responsible for reconfigurable signal routing. Our architecture, however, represents the first example of a system integrating nanoscale devices that combine both logic and programmability functions. These bottom-up nanowire circuits also have limitations in comparison with conventional CMOS circuits, although projections suggest that density, speed and power consumption can be further improved for our array architecture.

Area

The effective logic gate area in the unoptimized CTNW array demonstrated in this work is ~3.3 μm^2, which is larger than the logic gate area of 0.35 μm^2 in the present 32-nm CMOS generation.[33] We project that a CTNW logic gate area of 0.002 μm^2 is achievable, based upon estimates of dense packing of NW building blocks by Langmuir-Blodgett assembly[26] and reported scaling of charge-trapping devices.[29] This would be at least a 30-fold improvement over the 16-nm CMOS generation anticipated in 2016, which is projected[33] to feature a logic gate area of 0.063 μm^2 (Table 3-4). Our bottom-up assembly of CTNWs also enables the logic gates to be integrated in 3D stacking,[34] offering unique opportunities for even higher density of integration. We note that the state-of-the-art NAND flash memory,[29] another type of conventional CMOS

device, demonstrates an effective device area of 0.0015 μm^2 comparable to that of projected nanoprocessor. However, complex lithography and costly fabrication processes pose a significant challenge for scaling beyond the 22-nm technology node, whereas in our bottom-up approach critical dimension are not limited by lithography but rather defined by chemical synthesis and assembly.

Power consumption

The estimated power consumption of each NW logic gate is ~0.9 μW based on V_{DD} of ~3 V and on-state current of ~0.3 μA. This is larger than the 10-100 nW per gate consumed in 32-nm CMOS. However, with the introduction of complementary n-type NW devices[34], static power dissipation can be eliminated, leaving capacitive power and leakage as the primary sources of power consumption, and the projected CTNW logic gate power consumption may be reduced below 1 nW per gate. Specifically, the dynamic power consumption, W_D, of a capacitatively connected logic gate is given by

$$W_D = \alpha C {V_{DD}}^2 f$$

where α is the switching activity, C is the load capacitance, V_{DD} is the supply voltage, and f is the operating frequency. To assess the prospective power consumption of the programmable CTNW logic gates, we consider a simulated logic gate driving four other gates, i.e., a "fan-out of four" configuration (an industry standard for assessing logic gate performance in a technology-independent way). For this estimation, C is approximately 4 x 3.3 aF = 13.2 aF; V_{DD} is 3 V; f is 50 MHz. We note that the gate capacitance of 3.3 aF was estimated based on top-gate/NW geometry with the same gate dielectric thickness as the 2nm-2nm-5nm AZA stack of CTNW

(Fig. 3-12a). Typical switching activity in a large circuit is $\alpha = 0.1$. With these values, the estimate for dynamic power consumption is 0.6 nW. Static power consumption in a complementary logic gate is largely due to leakage. For the devices described here, the leakage current, i.e. off-state current, is approximately 20 pA (Fig. 3-12c). Thus, for a 3 V supply, the leakage power would be 60 pW per nanowire. For a small logic gate consisting of two or three nanowires, leakage power remains less than 200 pW per gate.

Switching speed

The prototype demonstrated in this work was developed to demonstrate correct static operation and was not optimized for maximum operating speed. In order to assess potential AC operation, we carried out circuit simulations for switching speed using the Cadence Design Framework II simulation environment[35]. Within this environment, an empirical device model[11] was developed where current vs. voltage curves generated by the model match quantitatively (e.g. 'on' current, 'off' current, threshold voltage, etc.) with the experimental results (Fig. 3-12b and c). Parasitic resistances and capacitances were also estimated based upon the physical composition of the wires and their geometry in relation to the substrate and each other; per unit CTNW junction cell, the parasitic resistance was estimated to be 2 Ω for metal electrodes and 70 KΩ for semiconducting NWs; capacitance to ground was estimated at 10 aF per cell; wire-to-wire coupling capacitance was estimated at 3 aF per cell. With these models and estimates for interconnect resistances and capacitances, simulations were performed for full-adder circuits. These simulations predict that for logic inputs switching between 0 and 3 V, output transients would settle to correct values in 5-10 ns, leading to an estimated top circuit speed of 100-200

MHz. A lower maximum speed of 50-100 MHz is projected if the simulated circuits were to be integrated into more complex logic. This is comparable to clock speeds required in real-time, low-power microcontrollers[36], an application of interest, but less than the 5 GHz achievable in conventional CMOS[33] for high-performance computing. It is noteworthy that Ge/Si NWFETs with 40 nm channel length have previously demonstrated intrinsic delay of 0.5 ps (or switching speed of 2 THz)[37], which defines an upper limit for Ge/Si NWFET-based logic operations. A summary of the present and projected key device area, power and speed metrics for our NW based logic tiles and CMOS are organized in Table 3-4 below:

Table 3-4 ***Comparison between present and projected bottom-up nanoprocessor and top-down CMOS systems****. Data for the 'Present Achievement' are extracted from experimental data shown in this work. 'Logic Gate Area' is calculated by the total device area (ca. 1620 μm^2, see Fig. 3-7b and c) divided by the total number of NWFET nodes (496). The total device area includes the top-gate array region (~960 μm^2), the S/D region containing 500-nm long metal contacts that align with the axes of the NWs, and two gap regions each consisting of ~500-nm wide gaps between the S/D and the top-gate array. 'Power Consumption' is estimated as described above. 'Projected Nanoprocessor' is modeled as an array with 6 CTNWs and 6 top-gates, both with 40-nm pitch, together with 20-nm long metal contacts to the ends of NWs and 20-nm wide gaps between S/D contacts and the top-gate array region. The gate pitch, composed of ~20 nm gate width and ~20 nm gap, is derived from state-of-the-art charge-trapping devices[29] and compatible with the lithography tools used in this study. The nanowire pitch is calculated based on demonstrated dense assembly[26] of NWs consisting of 10 nm diameter Ge NW core, 2 nm thick concentric Si shell, and conformal 12 nm charge-trapping layers. 'Logic Gate Area' is calculated*

Table 3-4 (Continued) by the total device area in this model (~0.07 μm^2) divided by the total number of NWFET nodes (36). 'Power Consumption' and 'Circuit Speed' are obtained by simulation as described above. Data for 'Present CMOS' and 'Projected CMOS' are obtained from Table ORTC-2C of the International Technology Roadmap for Semiconductor (ITRS).[33] The 'Logic Gate Area' in these cases contains the active channel, implanted S/D, area for contact plugs to S/D/G, and minimum spacing to adjacent transistors.

Metric	Present Achievement	Present CMOS (32 nm in 2010)	Projected Nanoprocessor	Projected CMOS (16 nm in 2016)
Logic Gate Area	3.3 mm^2	0.35 mm^2	0.002 mm^2	0.063 mm^2
Power Consumption	900 nW / logic gate	10-100 nW / gate	<1 nW / gate	10-100 nW / gate
Circuit Speed	Static tests to date	~5 GHz	50-100 MHz	~5 GHz

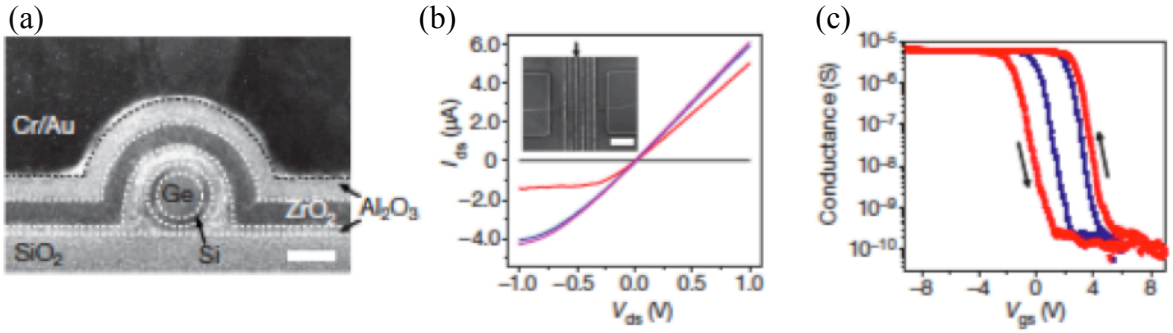


Figure 3-12 Structure and characterization of a typical programmable CTNWFET in the unit tile. (a), Cross-sectional transmission electron microscopy image of a representative nanowire device, with substrate surface (SiO_2) and gate (Cr/Au) at the bottom and the top of the image, respectively. Other components of the nanowire and dielectric layers are labeled, and dashed lines define the boundary between different components. Scale bar: 10 nm. (b), I_{ds}–V_{ds} curves recorded from a six-gate NWFET with V_{gs} = 8 (black), 3 (red), 0 (blue) and -8 V (magenta) (G3), and G1, G2, and G4–G6 grounded. Inset: scanning electron microscopy

Figure 3-12 (Continued) image of the device. The small black arrow indicates G3. Scale bar: 1 mm. (d), Semi-logarithmic plot of conductance versus V_{gs} for the same device as in (b), recorded for ±6V (blue) and ±9V (red) sweeps at V_{ds} = 0.5 V. The arrows represent sweep/hysteresis direction.

3.6 Conclusion

We have demonstrated a programmable and scalable architecture based on a unit logic tile consisting of two interconnected, programmable, non-volatile nanowire transistor arrays. Each NWFET node in an array can be programmed to an active or inactive transistor state, and by mapping different active-node patterns into the array, combinational and sequential logic functions including full-adder, full-subtractor, multiplexer, demultiplexer and D-latch were realized with the same programmable tile. Cascading this unit logic tile into linear or tree-like interconnected arrays, which we calculate will be possible given the demonstrated gain and matched input/output voltage levels of CTNWFET devices, provides a promising bottom-up strategy for developing increasingly complex nanoprocessors with heterogeneous building blocks.[34, 38] In the near term, particularly promising for this architecture and the low-power devices it contains are simpler, tiny, application-specific nanoelectronic control processors,[36] where such 'nanocontrollers' might make possible very small embedded electronic systems and new types of therapeutic devices.

Bibliography

1 Feynman, R.P. There's plenty of room at the bottom. *Engineering and Science* **23**, 22-36 (Caltech, February, 1960).

2 Haselman, M. & Hauck, S. The future of integrated circuits: a survey of nanoelectronics. *Proc. IEEE* **98**, 11-38 (2010).

3 Lu, W. & Lieber, C. M. Nanoelectronics from the bottom up. *Nature Mater.* **6**, 841-850 (2007).

4 Cui, Y. & Lieber, C. M. Functional nanoscale electronic devices assembled using silicon nanowire building blocks. *Science* **291**, 851-853 (2001).

5 Huang, Y., Duan, X., Cui, Y., Lauhon, L., Kim, K. & Lieber, C. M. Logic gates and computation from assembled nanowire building blocks. *Science* **294**, 1313-1317 (2001).

6 Zhong, Z. H., Wang, D. L., Cui, Y., Bockrath, M. W. & Lieber, C. M. Nanowire crossbar arrays as address decoders for integrated nanosystems. *Science* **302**, 1377-1379 (2003).

7 Bachtold, A., Hadley, P., Nakanishi, T. & Dekker, C. Logic circuits with carbon nanotube transistors. *Science* **294**, 1317-1320 (2001).

8 Javey, A. Kim, H., Brink, M., Wang, Q., Ural, A., Guo, J., McIntyre, P., McEuen, P., Lundstrom, M. & Dai, H. High-kappa dielectrics for advanced carbon-nanotube transistors and logic gates. *Nature Mater.* **1**, 241-246 (2002).

9 Borghetti, J., Snider, G. S., Kuekes, P. J., Yang, J. J., Stewart, D. R. & Williams, R. S. 'Memristive' switches enable 'stateful' logic operations via material implication. *Nature* **464**, 873-876 (2010).

10 DeHon, A. Array-based architecture for FET-based, nanoscale electronics. *IEEE Trans. Nanotechnol.* **2**, 23-32 (2003).

11 Das, S., Rose, G. S., Ziegler, M. M., Picconatto, C. A. & Ellenbogen, J. C. Architectures and simulations for nanoprocessor systems integrated on the molecular scale. *Lect. Notes Phys.* **680**, 479-513 (2005).

12 Dehon, A. Nanowire-based programmable architectures. *Acm. J. Emerg. Technol.* **1**, 109-162 (2005).

13 Lancaster, D. E. *TTL Cookbook (1st ed.)* (Sams, 1974).

14 Dehon, A. Design of programmable interconnect for sublithographic programmable logic arrays. *FPGA'05, Monterey*, California, USA (2005).

15 Dong, Y. J., Yu, G. H., McAlphine, M. C., Lu, W. & Lieber, C. M. Si/a-Si core/shell nanowires as nonvolatile crossbar switches. *Nano Lett.* **8**, 386-391 (2008)

16 Sheriff, B. A., Wang, D., Heath, J. R & Kurtin, J. N. Complementary symmetry nanowire logic circuits: Experimental demonstrations and in silico optimizations. *ACS Nano* **2**, 1789-1798 (2008).

17 Lu, W., Xiang, J., Timko, B. P., Wu, Y. & Lieber, C. M. One-dimensional hole gas in germanium/silicon nanowire heterostructures. *Proc. Natl. Acad. Sci. USA* **102**, 10046-10051 (2005).

18 Xiang, J., Lu, W., Hu, Y., Wu, Y., Yan, H. & Lieber, C. M. Ge/Si nanowire heterostructures as high-performance field-effect transistors. *Nature* **441**, 489-493 (2006).

19 Xiang, J., Vidan, A., Tinkham, M., Westervelt, R. M. & Lieber, C. M. Ge/Si nanowire mesoscopic Josephson junctions. *Nature Nanotechnol.* **1**, 208-213 (2006).

20 Javey, A., Nam, S., Friedman, R. S., Yan, H. & Lieber, C. M. Layer-by-layer assembly of nanowires for three-dimensional, multifunctional electronics. *Nano Lett.* **7**, 773-777 (2007)

21 Yu, G. & Lieber, C. M. Assembly and integration of semiconductor nanowires for functional nanosystems. *Pure Appl. Chem.* **82**, 2295-2314 (2010).

22 Duan, X., Huang, Y., Cui, Y., Wang, J. & Lieber, C. M. Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices. *Nature* **409**, 66-69 (2001).

23 Freer, E. M., Grachev, O., Duan, X., Martin, S. & Stumbo, D. P. High-yield self-limiting single-nanowire assembly with dielectrophoresis. *Nature Nanotechnol.* **5**, 525–530 (2010).

24 Huang, Y., Duan, X., Wei, Q. & Lieber, C. M. Directed assembly of one-dimensional nanostructures into functional networks. *Science* **291**, 630-633 (2001).

25 Jin, S., Whang, D., McAlpine, M. S., Friedman, R. S., Wu, Y. & Lieber, C. M. Scalable interconnection and integration of nanowire devices without registration. *Nano Lett.* **4**, 915-919 (2004).

26 Whang, D., Jin, S. & Lieber, C. M. Large-scale hierarchical organization of nanowires for functional nanosystems. *Jpn. J. Appl. Phys.* **43**, 4465-4470 (2004).

27 Yu, G. H., Cao, A. Y. & Lieber, C. M. Large-area blown bubble films of aligned nanowires and carbon nanotubes. *Nature Nanotechnol.* **2**, 372-377 (2007).

28 Fan, Z. Y. Ho, J. C., Jacobson, Z. A., Yerushalmi, R., Alley, R. L., Razavi, H. & Javey, A. Wafer-scale assembly of highly ordered semiconductor nanowire arrays by contact printing. *Nano Lett.* **8**, 20-25 (2008).

29 Sakamoto, W., Yaegashi, T., Okamura, T., Toba, T., Komiya, K., Sakuma, K., Matsunaga, Y., Ishibashi, Y., Nagashima, H., Sugi, M., Kawada, N., Umemura, M., Kondo, M., Izumida, T., Aoki, N. & Watanabe, T. Reliability improvement in planar MONOS cell for 20 nm-node multi-level NAND flash memory and beyond. *IEDM Tech. Dig.,* 831-834 (2009).

30 Sze, S. M. *Semiconductor Device – Physics and Technology* (John Wiley & Sons, 2002).

31 Sedra, A. S. & Smith, K. C. *Microelectronics Circuits* (Oxford Univ. Press, 2004).

32 Xia, Q. F., Robinett, W., Cumbie, M. W., Banerjee, N., Cardinali, T. J., Yang, J. J., Wu, W., Li, X., Tong, W. M., Strukov, D. B., Snider, G. S., Medeiros-Ribeiro, G. & Williams, R. S. Memristor-CMOS hybrid integrated circuits for reconfigurable logic. *Nano Lett*. **9**, 3640–3645 (2009).

33 *International Technology Roadmap for Semiconductors*, 2009 Edition. Available online at http://www.itrs.net

34 Nam, S., Jiang, X., Xiong, Q., Ham, D. & Lieber, C. M. Vertically integrated, three-dimensional complementary metal-oxide-semiconductor circuits. *Proc. Natl. Acad. Sci. USA*, **106**, 21035-21038 (2009).

35 Cadence Design Framework II, Version IC 5.1.41. Cadence Design Systems, San Jose, CA.

36 Das, S., Gates, A. J., Abdu, H. A., Rose, G. S., Picconatto, C. A. & Ellenbogen, J. C. Designs for ultra-tiny, special-purpose nanoelectronic circuits. *IEEE Trans. Circuits Syst. Regul. Pap.* **54**, 2528-2540 (2007).

37 Hu, Y. J., Xiang, J., Liang, G. C., Yan, H. & Lieber, C. M. Sub-100 nanometer channel length Ge/Si nanowire transistors with potential for 2 THz switching speed. *Nano Lett.* **8**, 925-930 (2008).

38 Lu, W., Xie, P. & Lieber, C. M. Nanowire transistor performance limits and applications. *IEEE Trans. Electron. Dev.* **55**, 2859–2876 (2008).

Part II : Looking into the NWFET biosensor: critical components and qualifying factors for sensing

Chapter 4

Understanding NWFET biosensor and surface modification

Nanotechnology has progressed dramatically in recent decades with the development of zero-dimensional structures (metallic nanoparticles,[1] semiconductor nanoparticles,[2] and magnetic nanoparticles[3]), one-dimensional structures (carbon nanotube,[4] semiconductor nanotube,[5] semiconductor nanowire,[6-8] metallic nanowire[9]), and two-dimensional structures (graphene,[10] nanopore,[11] metal film,[12] and nanostructured surface film[13]). These novel nanostructures have been implemented for use as molecular biosensors,[14] bioprobes,[15-17] and other nanosystems capable of diagnostics due to their high sensitivity and performance. The large surface area-to-volume ratio of nanostructures enables the amplification of signals induced by target bio-molecules because physical and chemical effects on the surface of nanosystem critically dominate states of the biosensor device.[18, 19]

Biosensors can be classified by their method of signal transduction. These include (1) optical detection methods based on fluorescence,[20] Raman,[21] surface-enhanced Raman,[22, 23] refraction/dispersion, phosphorescence spectroscopy,[24] (2) Mass-change detection methods based on piezoelectric resonator[25] and quartz crystal microbalance(QCM),[26] and (3) electrochemical detection methods based on field-effect transistor (FET)[27, 28] and screen-printed

metal electrodes.[29] Compared to other biosensors, the nanoscale FET offers significant advantages for real-time, highly sensitive, multiplexed and label-free electrical detection, even though FET-based biosensors lose sensitivity as ionic strength of the solution increases, a common issue for electrochemical sensors based on charge detection.[30] The ions in a high ionic strength solution screen the charges of the target analyte and neutralize them such that when it is located at a distance beyond the Debye length the electrochemical biosensor loses the ability to sense it. Understanding the FET biosensor system and analyzing its limitations are therefore necessary not only to improve and optimize its function but also to overcome its limitations in the design of a novel biosensor that may be used under physiological conditions.[31]

Semiconductor nanowire building blocks are one of the best candidates for a novel FET biosensor. Developments in nanowire growth have led to the demonstration of a wide range of nanowire materials with precisely controlled size,[6] structure,[7, 8] morphology,[32] and composition[7, 8, 33-35] and capable of property modulation. The controllability of nanowire building blocks allows us to produce a nanoscale FET with a single-crystal-based cylindrical structure.[6] Furthermore, a molecular-scale nanowire FET has been demonstrated which has very high surface-to-volume ratio (3 nm diameter cylindrical nanowire: 1.67 nm^{-1}, in other words, ~67%).[36] In the case of bulk FET devices, a charged target molecule bound on the surface can only modulate a number of majority carriers within a few nanometers, because the screening length in semiconductors, λ_{semi}, is a few nanometers (i.e. 1~2nm for silicon with a hole density of 10^{18}~$10^{19}/cm^3$.[37] By contrast, the high surface-to-volume ratio and small diameter in the nanowire FET allows the surface potential charge on the semiconductor nanowire to dominate

conductance changes along the FET channel even with the short screening length of semiconductor; this results in sensitive detection of charged molecules.[38]

In this chapter, I describe an innovative biomolecular sensing probe created by modulations of structure and dopants, discuss the theoretical analysis of semiconductor nanowire field-effect transistor (NWFET) sensitivity in low ionic strength solution and explore the experimental analysis of functionalization and antibody modification on the surface of the device.

4-1. Theoretical sensitivity of NWFET biosensor in low ionic strength solution

The NWFET is a nanoscale three-terminal switch modulated by a gate potential. This 1D system can transduce an electrochemical reaction on its surface into an electrical signal correlated to conductance of NWFET channel by field effect. Its high electrical performance with large surface-to-volume ratio as well as high capacitive coupling through a thin native gate oxide enables an enhanced sensitivity for charged biomolecules. In this section, I discuss the specific charge sensitivity of a NWFET biosensor in a direct current (DC) measurement as a simple model to introduce the fundamentals of the conventional system, and move forward to a new concept of NWFET biosensors for the future.

Fig. 4-1a depicts a normal biosensing environment composed of a NWFET, chemical layers on the NWFET surface for specific binding/unbinding of target analytes, target biomolecules, and ionic solution. We assume that: (1) the NWFET is an ideal cylindrical structure of silicon (Si) with 1 nm conformal SiO_2 gate oxide, (2) the solution is electrically neutral, (3) the target molecules can be considered point-charges, and (4) the solution potential is

constant. The main purpose of calculating the change in NWFET conductance by charges over its surface is to figure out the screening effect of those charges in ionic solution.

Because the solution is neutral,

$$\sum_{i=0}^{n} N_i z_i = 0 \tag{4-1}$$

is valid, where N_i is the total number of ions of species i in the solution and z_i is the charge number of species i. Because the solution potential is constant, the ions are in thermal equilibrium with each other and act as free charges. This means that they follow Boltzmann statistics such that

$$n_i = \frac{N_i}{V} e^{-\frac{z_i q \varphi}{k_B T}} \tag{4-2}$$

at all points in the solution, where n_i, V, q, φ, k_B, and T are the number density of all species, volume of the solution, an elementary charge, electrical potential, Boltzmann constant, and absolute temperature respectively. Therefore, the charge density in the solution is

$$\rho = \sum_{i=0}^{n} q n_i z_i = \sum_{i=0}^{n} q z_i \frac{N_i}{V} e^{-\frac{z_i q \varphi}{k_B T}} \tag{4-3}$$

from equation (4-1) and (4-2). In order to calculate electrical potential in the solution, we can use the Poisson equation[39] as follows:

$$\nabla^2 \varphi = -\frac{\rho}{\varepsilon_r \varepsilon_0} = -\frac{1}{\varepsilon_r \varepsilon_0} \sum_{i=0}^{n} q z_i \frac{N_i}{V} e^{-\frac{z_i q \varphi}{k_B T}} \tag{4-4}$$

where ε_r and ε_0 are relative and vacuum permittivity respectively. For a high ionic strength solution, it is difficult to solve eq. 4-4 due to non-linearity of the differential equation. However,

for a low ionic strength solution z should be small, and the exponential part can be treated linearly by a first order of Taylor series. Hence, equation (4-4) becomes

$$\nabla^2\varphi = -\frac{1}{\varepsilon_r\varepsilon_0}\sum_{i=0}^{n} qz_i\frac{N_i}{V}e^{-\frac{z_iq\varphi}{k_BT}} = -\frac{1}{\varepsilon_r\varepsilon_0}\sum_{i=0}^{n} qz_i\frac{N_i}{V}\left(1-\frac{z_iq\varphi}{k_BT}\right)$$

$$= -\frac{1}{\varepsilon_r\varepsilon_0}\sum_{i=0}^{n} qz_i\frac{N_i}{V} + \frac{1}{\varepsilon_r\varepsilon_0}\sum_{i=0}^{n}\frac{N_i}{V}\cdot\frac{{z_i}^2q^2\varphi}{k_BT} = \frac{1}{\varepsilon_r\varepsilon_0}\sum_{i=0}^{n}\frac{N_i}{V}\cdot\frac{{z_i}^2q^2\varphi}{k_BT} \qquad (4\text{-}5)$$

From eq. (4-1) $\left(\frac{q}{V}\sum_{i=0}^{n} N_i\, z_i = 0\right)$

From general definition of ionic strength of the solution

$$I = \frac{1}{2}\sum_{i=0}^{n}\frac{N_i}{V}{z_i}^2 \qquad (4\text{-}6)$$

so that eq. (4-5) is

$$\nabla^2\varphi = \frac{1}{\varepsilon_r\varepsilon_0}\sum_{i=0}^{n}\frac{N_i}{V}\cdot\frac{{z_i}^2q^2\varphi}{k_BT} = \frac{2Iq^2\varphi}{\varepsilon_r\varepsilon_0k_BT} = \kappa^2\varphi \qquad (4\text{-}7)$$

This is the solvable form of the Helmholtz equation where $\kappa^{-1} = \sqrt{\frac{\varepsilon_r\varepsilon_0k_BT}{2Iq^2}}$ is defined to Debye screen length[40]. The equation may be expressed in spherical coordinates by taking r = 0 at some arbitrary ion. Therefore, the general solution of Helmholtz equation in spherical coordinate[41] will be

$$\varphi(r) = A_1\frac{e^{-\sqrt{\kappa^2}r}}{r} + A_2\frac{e^{\sqrt{\kappa^2}r}}{2r\sqrt{\kappa^2}} = A_1\frac{e^{-\kappa r}}{r} + \frac{A_2}{2\kappa}\frac{e^{-\kappa r}}{r} \qquad (4\text{-}8)$$

where A_1 and A_2 are arbitrary constants. Note that r is the distance from the charge source in ionic solution (Fig 4-1a). From boundary conditions, the potential should be 0 if r is infinite, so that A_2 should be zero.

$$\therefore \varphi(r) = A_1 \frac{e^{-\kappa r}}{r} \tag{4-9}$$

We assumed that the charges are considered points and surrounded by ions. Inside the screened space, ions should follow

$$\therefore \varphi(r) = \frac{Q}{4\pi\varepsilon_r\varepsilon_0 r} \tag{4-10}$$

according to Gauss's law, where Q are all charges in the center. If r is very small,

$$A_1 \frac{e^{-\kappa r}}{r} \Longrightarrow \frac{Q}{4\pi\varepsilon_r\varepsilon_0 r}$$

$$\therefore A_1 = \frac{Q}{4\pi\varepsilon_r\varepsilon_0} \tag{4-11}$$

Therefore, the induced potential by charge Q in low ionic strength solution at a large distance from the center is

$$\varphi(r) \cong \frac{Qe^{-\kappa r}}{4\pi\varepsilon_r\varepsilon_0 r} \tag{4-12}$$

This means that the amount of charge Q will equal the amount of charges as $Qe^{-\kappa r}$ at the point r.

For the system of NWFET biosensor, consider a p-type NWFET which has an antibody-modified surface; the potential charges on the oxide surface of NWFET by the antigen-antibody pair can be calculated by

$$\Delta V_G = \frac{Q_S}{C_{oxide}} = \frac{Q_A e^{-\kappa r_0}}{C_{oxide}} \times [Antibody] \frac{\alpha[Antigen]}{1 + \alpha[Antigen]} \tag{4-13}$$

where '[ ]' denotes concentration and Q_A, C_{oxide}, r_0 and α are charges by antigens, capacitance of gate oxides per length, distance from the antigen layer to oxide layer, and the equilibrium constant. It is worth noting that the second term is the total number of antigen-antibody complex based on Langmuir adsorption equation[42] and the antibody layer is formed at distance r_0 from the surface of NWFET. In addition, bringing the linear operation of NWFET from eq. (1-5), the current change by bound antigens is

$$\Delta I_{DS} = \frac{1}{L^2}\mu C_{ox}(\Delta V_G \cdot V_{DS})$$

$$= \frac{1}{L^2}\mu\left(Q_A e^{-\kappa r_0} \times \frac{[Antibody]}{l} \cdot \frac{\alpha[Antigen]}{1+\alpha[Antigen]}\right) \quad (4\text{-}14)$$

Now, considering the specific parameters of the system as in Table 4-1, assuming $[\text{Antigen}] >> \frac{1}{\alpha} = K_D$, which means that all antibody-sites are occupied by antigens, the top-gate potential changes due to a singly-charged antigen simplifies as

$$\Delta V_G = \frac{Q_A e^{-\kappa r_0}}{C_{oxide}} \times [Antibody] \quad (4\text{-}15)$$

This result shows the NWFET sensitivity for the charged antigen bound to the antibody layer in solutions of varying ionic strength and different antigen charge numbers. For example, the gate potential change by 100 antigen-antibody complexes per μm on a 30 nm-diameter NWFET is ~4.8 mV in 1 μM ionic strength solution shown as Fig. 4-2. Fig. 4-2 based on eq. (4-15) shows the significant effect of ionic strength on ΔV_G induced by a single charge in the target antigen

Table 4-1 Main parameters used for the simulation in Fig. 4-1b

Main parameter	**Values**
Diameter of SiNW(r_{core})	30nm
SiO2 thickness of gate oxide (t_{oxide})	1nm

Table 4.1

Table 4-1 (Continued)

Gate oxide capacitance of SiNW	$\sqrt{\frac{2\pi\times\varepsilon_{SiO_2}\times\varepsilon_0}{\ln\frac{r_{core}+t_{oxide}}{r_{core}}}} = 3.36nF$
Distance between antigen binding point and NWFET surface (r_0)	10nm
Ionic strength of solution (I)	1μM
Antibody concentration ([Antibody])	100 / μm

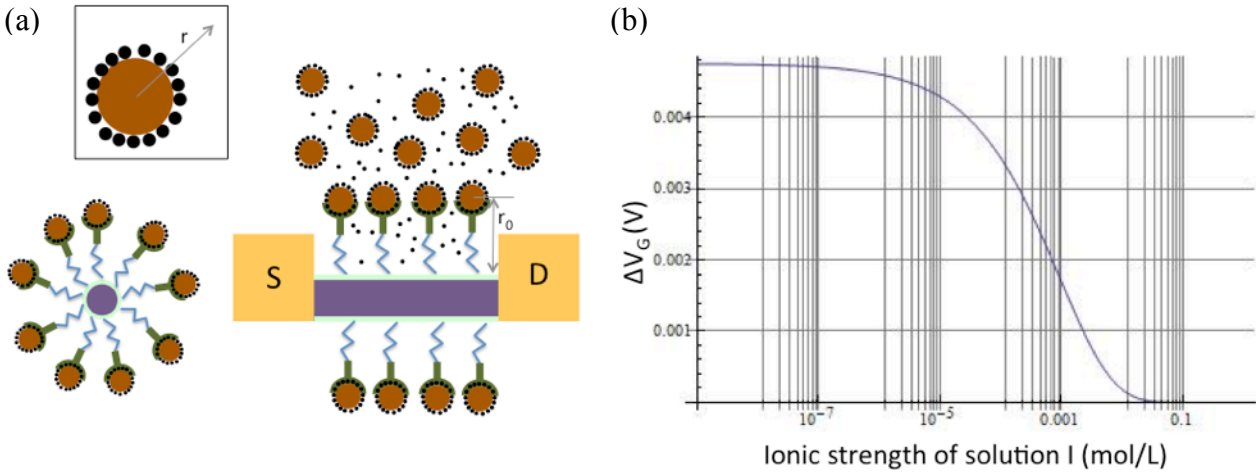


Figure 4-1 Model and model result for NWFET sensitivity. (a), Schematics of simulated system of NWFET biosensor modified by antibody for detection of target antigens. Red circle, black circle, and Y shape with a wavy line represent a charged antigen, an ion in solution, and a chemically modified antibody respectively. Cross-sectional view of NWFET biosensor (left) shows clear semiconducting nanowire (purple circle)/gate oxide (cyan ring) core/shell nanowire structure with antigen-antibody complexes on the surface of NWFET. Front view of NWFET (right) shows that the binding point of antigen on antibody is located at r_0 distance from the gate of NWFET. Inset: typical structure of charged antigen in solution of a given

Figure 4-1 (Continued) ionic strength. Note that the charged antigen is surrounded by oppositely charged ions so that its potential is screened. (b), Curve of potential changes by target antigen binding vs. ionic strength of solution in NWFET biosensor in system (a). Significant screening effect of electrical potential by background ions is simulated over 10 μM range of solution ionic strength.

4-2. Rational synthesis of kinked NWFET for a biochemical sensing probe

The FET device has many advantages as a biosensor, such as its high input impedance, and high sensitivity due to FET gain. Also, the nanoscale structure is non-invasive in a biological system in which the device is smaller than one of the smallest units of the system. These unique strengths of the nanoscale FET open up truly new opportunities for the investigation of living organisms.

Specifically, a FET based on nanowire building blocks is a powerful candidate to probe biological systems because its production via the bottom-up approach allows controllable synthesis. Recently, a method for synthesis of single crystalline kinked semiconducting nanowire superstructures was developed, and these structures were successfully implemented as minimally invasive three-dimensional (3D) NWFET bioprobes for intracellular electrical recording.[15] This superstructure utilizes the p-n junction FET (JFET), which is capable of highly localized electrical sensing in the cell.[43]

The success of a kinked nanowire platform for electrical recording in the cell motivates us to think about a new biosensor concept: a 3D biomolecular/chemical sensing probe for

intracellular research such as proteomics (Fig 4-2). Conventional FET-based biosensors require delivery of analytes to the devices, which is one of the biggest barriers to progress for *in vivo* research.[31] By contrast, the active probe-type NWFET can electrically detect target proteins with high-resolution tracking of the device position by simultaneous intracellular monitoring of its photocurrent[44] in real time. In this section, I discuss the synthesis, fabrication and the characterization of n++/intrinsic (i)/n++ kinked nanowire FET for the future generation of 3D intracellular biomolecular sensors.

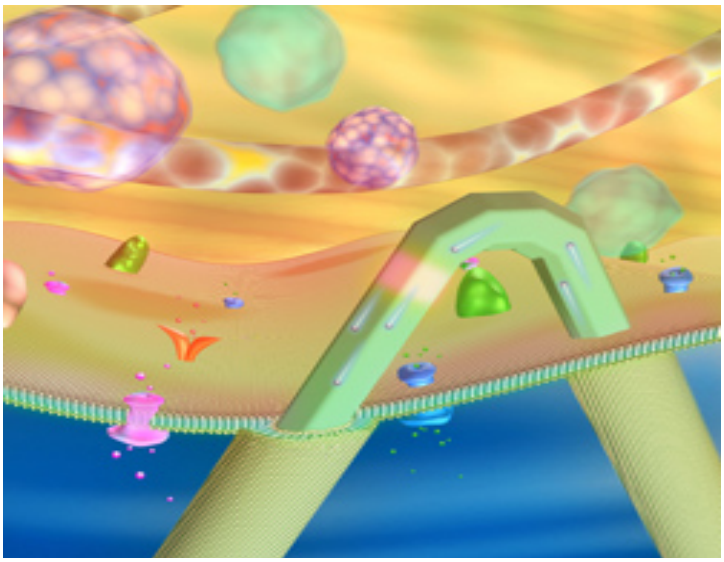


Figure 4-2 Schematic of a concept of 3D biomolecule / chemical sensing probe for intracellular researches based on kinked NWFET. Courtesy of Ref. [45]

The growth of kinked semiconducting nanowire with dopant modulation by the CVD-VLS method starts with the preparation of 80-nm Au catalyst substrate as introduced in Section

1.2. In the first stage, heavily doped n-type “arm” is grown by delivering 1 sccm SiH_4, 4 sccm PH_3 (1,000 ppm in H_2), and 60 sccm H_2 to the Au catalyst substrate for 25 min at a total pressure of 40 Torr and temperature of 455 °C. To form the kinked point in the arm, growth is paused for 15 s by shutting off all gas lines and simultaneously evacuating the chamber to its lowest pressure. 1 sccm SiH_4, 4 sccm PH_3 (1,000 ppm in H_2), and 60 sccm H_2 are then reintroduced to the growth substrate for 2 min at the same total pressure and temperature as previously. Shutting off only the PH_3 gas line for 1 min at this point allows the synthesis of ~500-nm intrinsic silicon nanowire. 4 sccm PH_3 was delivered again for 2 min with 1 sccm SiH_4 and 60 sccm H_2, at the same total pressure and temperature. A second evacuation of 15 s follows. In the final stage, the heavily doped n-type arm is grown for 15 min under the same conditions as the first stage (Fig. 4-3b). Fig. 4-3a shows a schematic of the expected NW grown by this method, and Fig. 4-3c, d, and e show optical, SEM, and high resolution TEM (HRTEM) images, respectively, of typical grown kinked n++ / i / n++ nanowire corresponding to the expected NW structure following the growth procedure. The HRTEM images reveal the single-crystallinity and smooth surface boundary of the kinked nanowire. The short semiconducting channel, in contrast to heavily doped arms, can be successfully defined and recognized as the region between the first and second kinked point.

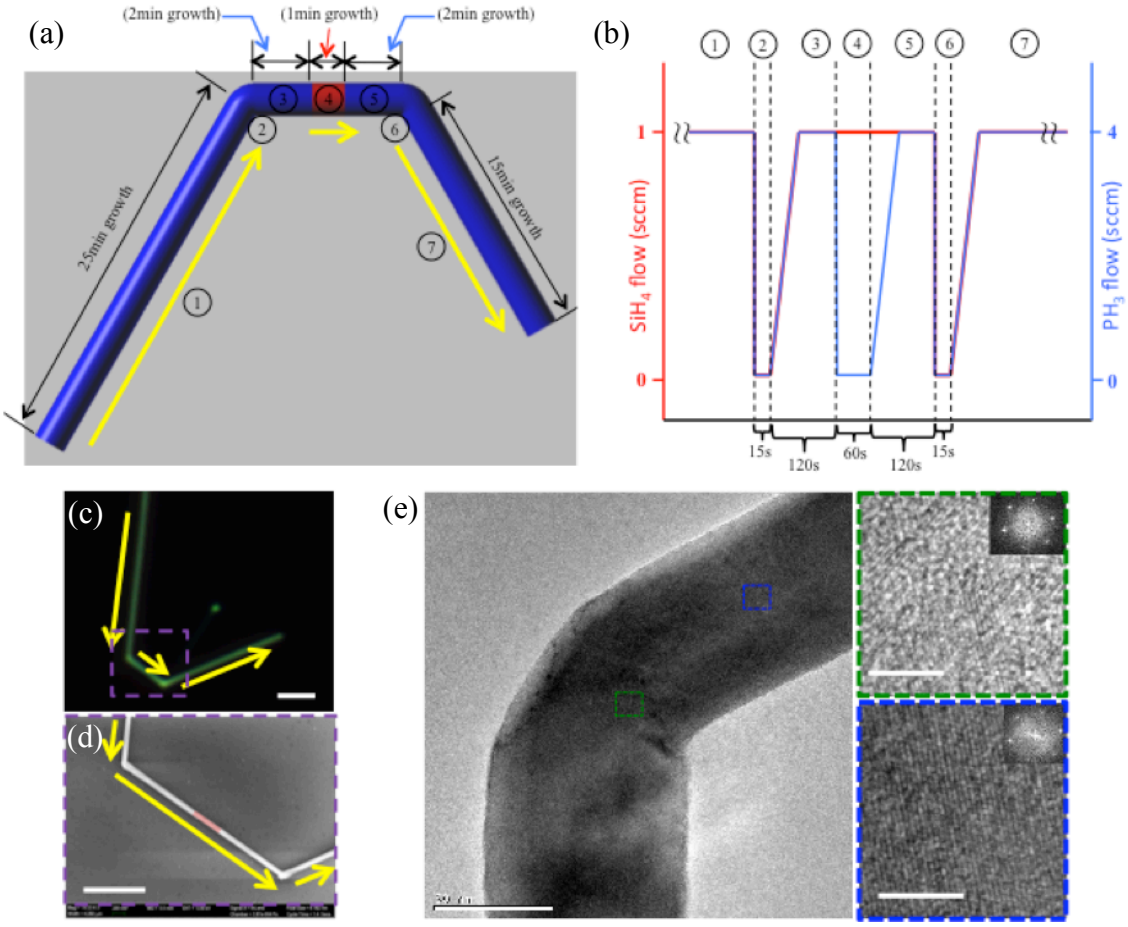


Figure 4-3 Synthesis of n++/ i / n++ kinked nanowire. (a), Schematic of the structure of n++/ i / n++ kinked nanowire. Yellow arrows and circled numbers indicate growth direction and order respectively. The blue and red colors of the nanowire body correspond to the heavily n-doped (n++) and intrinsic (i) parts. (b), SiH_4 and PH_3 flow during NW growth. The circled numbers match the ones in (a). The pause in the supply of precursors generates the kinked points. (c), Dark-field optical microscope image of a typical kinked nanowire. Yellow arrows indicate growth direction. Scale bar: 3 μm. (d), SEM image of the kinked nanowire in (c). The area shown corresponds to the purple dashed box in (c). Yellow arrows indicate growth direction and false red coloring indicates the intrinsic part estimated from the growth conditions. Scale bar: 1 μm. (e), HRTEM imagse of kinked nanowire. The image of kinked

Figure 4-3 (Continued) part (upper right, green dashed box, scale bar: 5 nm) and straight part (lower right, blue dashed box, scale bar: 5nm) reveals single crystallinity. Upper right inset and lower right inset show fast fourier transform (FFT) image which are recorded along the $[\bar{1}11]$ *zone axis.*[46]

Following synthesis, the kinked nanowires are drop-casted from the growth substrate onto a pre-defined marker substrate for further fabrication. The typical yield of kinked nanowires on the drop-casted substrates is ~40%. The transferred NWs are converted into FETs through position registry, EBL, and source/drain metallization, using the same procedures of straight NWFET fabrication provided in Section 2-3. To isolate the metal electrodes of the NWFET from the solution, SU-8 was applied by EBL as a passivation layer.

Fig 4-4 shows the I_{ds}-V_{ds} curves and water-gate (V_{WG}) performance of a typical n++/i/n++ kinked nanowire FET in PBS 1 mX with Ag/AgCl electrode. The device has an ohmic contact and the gate response of n-type FET with ~10,000 nS of transconductance. Interestingly, the transconductance-to-noise ratio of the device indicates the sensitivity is ~5,000, so that the minimum detectable potential change on the gate is >0.2mV. The theoretical results from Section 4-1 indicate that the device sensitivity is sufficient to detect five antigen-antibody complexes (if each antigen carries a single charge). In the next section, I will discuss surface modification of the SiNW to produce the NWFET biomolecular sensor.

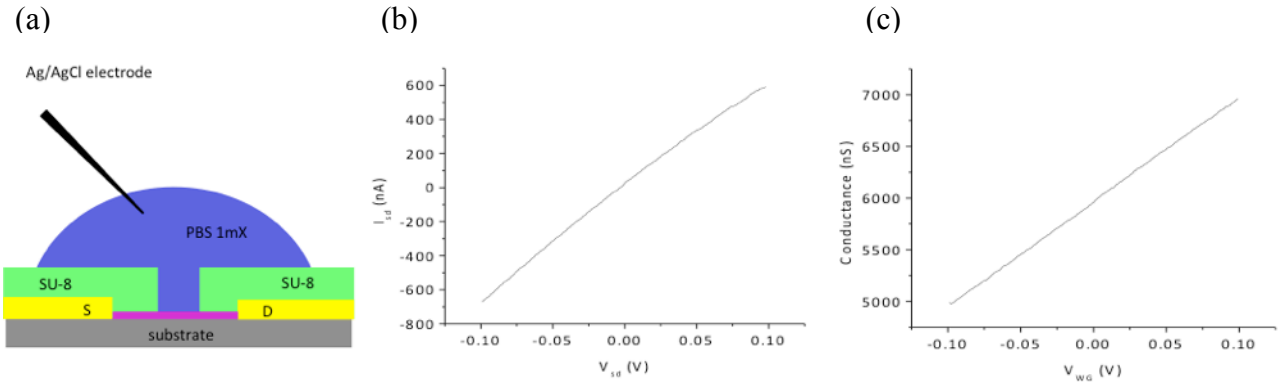


Figure 4-4 Characteristics of n++/i/n++ kinked NWFET in solution. (a), Schematic of the system of water-gate characterization for (b) and (c). Note that the potential of PBS 1 mX is controlled by a Ag/AgCl electrode and the only channel of kinked NW (pink) is exposed to PBS 1 mX. (b), I_{ds} vs. V_{ds} curve of kinked NWFET at V_{WG} = 0V (c), conductance vs. V_{WG} curve of kinked NWFET at V_{ds} = 0.1

4-3 Analysis of surface functionalizations on SiNW

In general, there are two main strategies to covalently bind either ligand or antibody to the SiNWFET. We take advantage of the fact that the protein's primary structure is composed of a specific series of amino acids which have amino and carboxyl chemical functional groups.[47] An aldehyde group forms an imine group when it reacts with an amine group by nucleophilic addition in an acidic buffer. Alternatively, an amine group can react with a carboxyl group with the help of 1-ethyl-3-(3-dimethylaminopropyl) carbodiimide (EDC) and N-hydroxysuccinimide (NHS), forming amides.[48] Hence, in order to generate aldehyde- or amino-terminated silicon oxide surfaces, we use the following typical approaches.

First, (3-aminopropyl)triethoxysilane (APTES) and glutaraldehyde (GA) are employed as shown in Fig. 4-5. Starting with O_2 plasma treatment (0.5 Torr, 40 W, 1 min) on the SiNW surface for termination of hydroxyl groups, 1% v/v APTES in 95% ethanol solution is applied for 45 min at room temperature, followed by gentle rinsing with IPA, a flow of nitrogen to dry, and baking at 115^{o}C for 5 min. It should be noted that the baking process can increase cross-linking of APTES. The APTES-modified SiNW is soaked in 2.5% GA and 6 mM $NaBH_3CN$ solution in PBS 1X (pH 7.9) for two hours. The modification process is completed by rinsing the SiNW with water, acetone, and IPA and drying under a gentle flow of nitrogen. The NW surface is now functionalized with aldehyde groups. To modify these with antibody, ultrafiltrated 100 µg/mL antibodies (14,000 x g (acceleration of gravity) for 15 min) are prepared with 6 mM $NaCNBH_3$ (reducing agents) in 10 mM phosphate buffer (PB), pH 8.4, followed by application to the substrate for two hours.

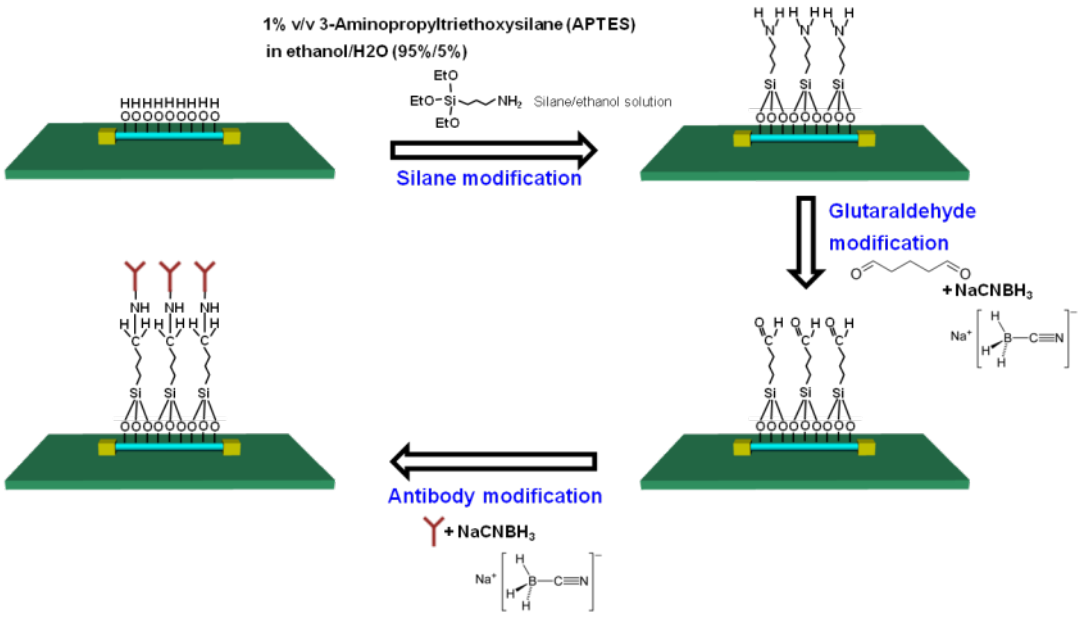


Figure 4-5 Schematic of SiNW (cyan color) surface modification with APTES and GA to covalently attach antibodies.

Second, 3-(trimethoxysilyl)butyl aldehyde (TBA) can be used as in Fig. 4-6. In principle, TBA, which has three terminal methoxy groups similar as APTES as well as an aldehyde group like GA, is superior to APTES + GA in terms of Debye length in ionic solution, because the total chemical chain length is ~2 nm shorter. After O_2 plasma treatment (0.5 Torr, 40 W, 1 min), the SiNW is immersed in 1% TBA in 95% ethanol solution for 45 min at room temperature. The NW is gently rinsed by ethanol and dried in a flow of nitrogen followed by baking at 110^{o}C for 10 min. Subsequent antibody modification is the same as described in the APTES+GA modification.

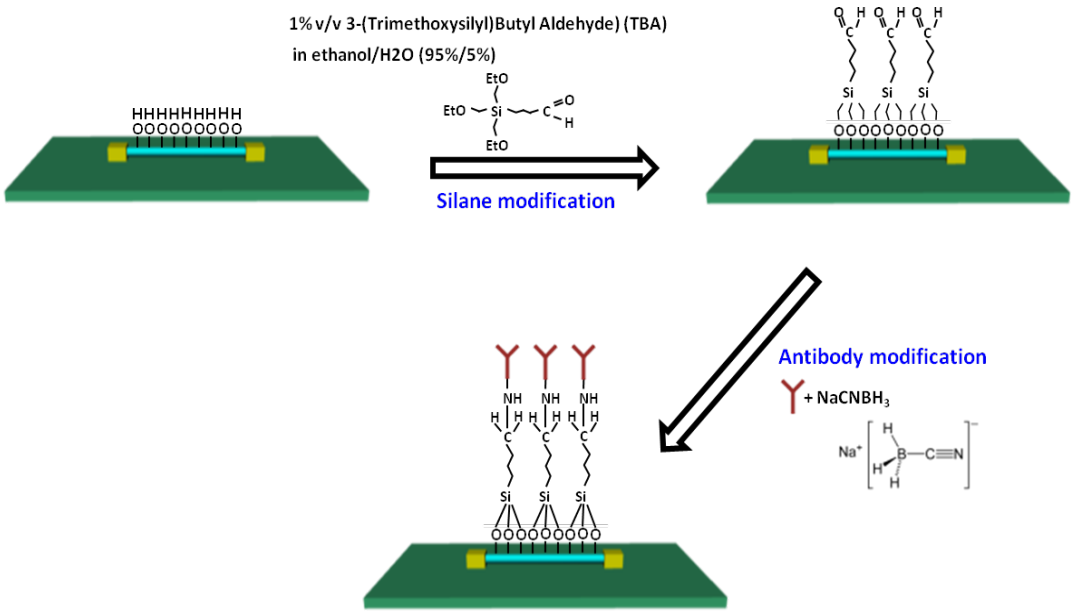


Figure 4-6 Schematic of SiNW (cyan color) surface modification with TBA to covalently attach antibodies.

Lastly, as shown in Fig. 4-7, APTES and EDC/NHS can be applied to use carboxyl groups on proteins unlike the others in using amino groups. All processes up to APTES

modification are the same as the first approach. A mixture of 4 mM EDC and 5 mM NHS in activation buffer (0.1 M 2-(N-morpholino)ethanesulfonic acid (MES), 0.5 M NaCl, pH 6) containing 100 ug/mL antibodies is drop-casted onto the APTES-modified SiNW for two hours at room temperature followed by rinsing with deionized (DI) water and drying under a flow of nitrogen.

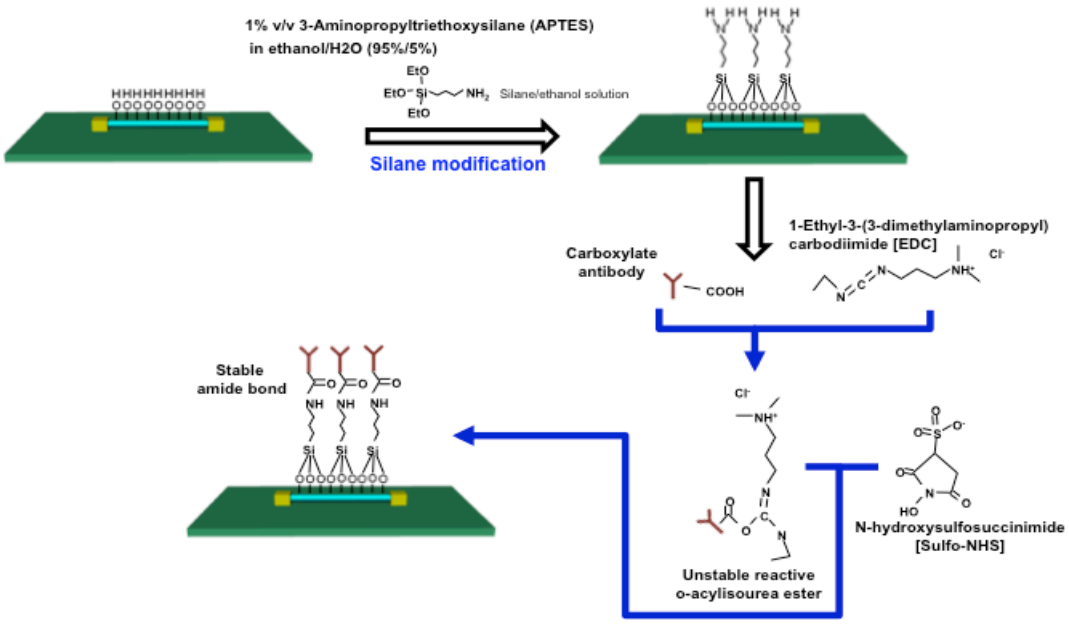


Figure 4-7 Schematic of SiNW (cyan color) surface modification with APTES and EDC/NHS to covalently attach antibodies.

The success of surface modification by the three approaches can be qualitatively and quantitatively confirmed by surface chemical analysis techniques such as a contact angle measurement and X-ray photoelectron spectroscopy (XPS) and attenuated total reflectance mode - Fourier transform infrared spectroscopy (ATR-FTIR). First, tracking the contact angle, which reflects wettability of the surface, can provide a qualitative view of whether the chemical

layer has been successfully generated after surface modification.[49] We expect the contact angle to be changed after surface modification because all the modification processes transform hydroxyl-terminations by O_2 plasma treatment to either aldehyde or amino terminations. Second, XPS can quantitatively measure the composition and chemical/electronic state of the elements on the surface (top 1 ~ 10 nm) of material. When a homogeneous X-ray beam hits and interacts with a material under ultra-high vacuum conditions ($<10^{-7}$ Torr), both scattering and fluorescent radiation occur, which are closely correlated with the atomic weight of the components.[50] Hence, measuring the kinetic energy and number of escaping electrons generates surface chemical information during X-ray irradiation of the target material. Third, ATR-FTIR enables identification of existing functional groups and examination of the chemicals on the surface. Measurement of absorbed infrared light, whose origins are the translational and vibrational energy of the bond or group, from the IR-irradiated material can reveal particular information about functional groups on the modified substrate.[51]

To simplify experiments, contact angle measurement was performed on similarly modified n-Si (100) wafers, which have the same native silicon dioxide surface properties as SiNW. Fig. 4-8 shows the results at the stage directly following O_2 plasma treatment, APTES modification, and APTES+GA modification. As expected, APTES- and APTES+GA-modified Si wafer demonstrate a higher contact angle; in other words they are more hydrophobic than hydride Si wafer. This is qualitative evidence that chemical layers are being deposited through either the APTES or GA modification process. Reported contact angles of both APTES[52] and GA[53] are in the range of 40-70 degrees, which agrees well with our results, though the success of GA modification on top of APTES modification cannot be assessed by this method.

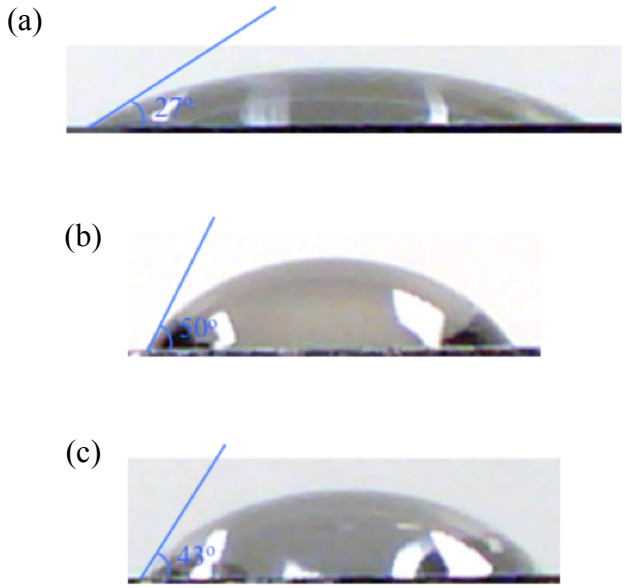


Figure 4-8 Results of contact angle measurement after oxygen plasma treatment, APTES modification, and GA modification. (a), Hydride Si wafer by oxygen plasma treatment. Contact angle: 27°. (b), APTES-modified Si wafer. Contact angle: 50°. (c), APTES+GA-modified Si wafer. Contact angle: 43°.

Additionally, XPS (K-Alpha, Thermo Scientific) analysis was done on surface-modified n-Si (100) wafer under various conditions to quantify the success of chemical modification. Because the Si surface modified by APTES, GA, and TBA is terminates in amino and aldehyde groups, it is mainly the binding energy range of C1s and N1s that is analyzed. Fig. 4-9a-d show the XPS results of pristine, APTES-modified, APTES+GA-modified, and TBA-modified Si wafer, respectively. For pristine bare Si (Control), a high C-C bond count per second (CPS) was observed, though the value is one order of magnitude less than in the case of APTES,

APTES+GA and TBA modification. This abnormality may result from carbon contamination by carbon dioxide in air because nitrogen s1 shows only baseline noise CPS. Compared to the control, both APTES- and APTES+GA-modified surfaces reveal C-C, C-N, NH_2, and NH_3^+ bonds (by CasaXPS^{TM} ver. 2.3.16, Casa Software Ltd.). Peak fitting for carbon 1s shows two peaks resolved for only the APTES-modified sample, due to C-C and C-N, whereas for the sample further treated with GA an additional C=O peak is resolved at higher energy, suggestive of surface aldehyde groups. Consistently, the C-N intensity decreases after GA modification, as would be expected if additional carbon chains cover the nitrogen of the APTES surface. C-C increases in intensity also, presumably due to additional carbon chains. Examination by XPS of the TBA-modified surface shows C-O/C=O and C-C bonds from peak fitting in carbon s1 and non-bond related to nitrogen s1, which are expected results from TBA chemical structure. Therefore, these XPS results reveal that the APTES-modified, APTES+GA-modified, and TBA-modified Si wafer is well-functionalized by aldehyde groups or amino groups as expected.

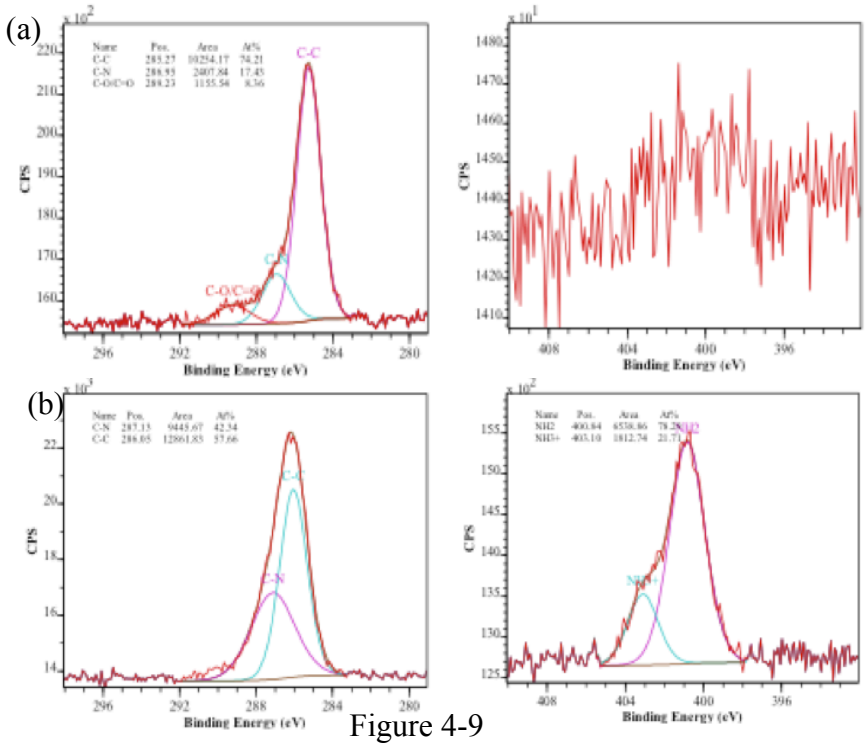


Figure 4-9

Figure 4-9 (Continued)

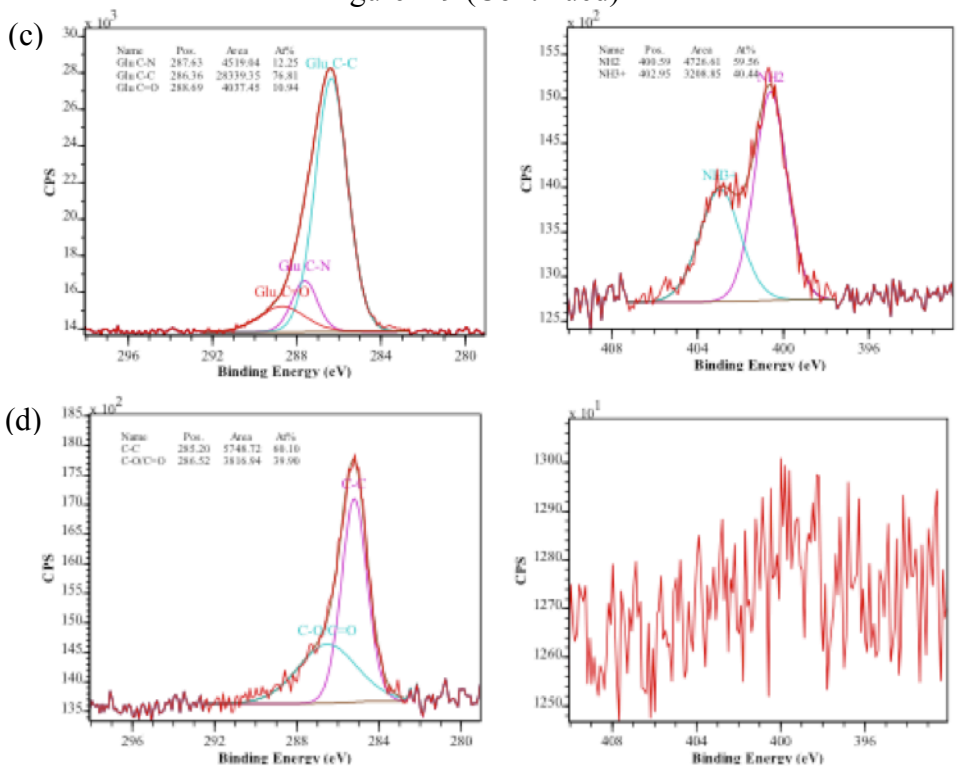


Figure 4-9 High-resolution XPS spectra of various functionalized surfaces. (a), C1s (left) and N1s (right) peaks of binding energy of pristine bare Si wafer. The C1 peak in the left curve is fitted to the binding energy of C-C, C-N, and C-O/C=O bonds. (b), C1s (left) and N1s (right) peaks of binding energy for the APTES-modified Si wafer. The C1 peak in the left curve is fitted to the binding energy of C-C and C-N bonds. The N1 peak in the right curve is fitted to the binding energy of NH_3^+ and NH_2. (c), C 1s (left) and N 1s (right) peak of binding energy of APTES+GA-modified Si wafer. The C1 peak in the left curve is fitted to the binding energy of C-C, C-N, and C=O bonds. The N1 peak in the right curve is fitted to the binding energy of NH_3^+ and NH. (d), C1s (left) and N1 (right) peak of binding energy of TBA-modified Si wafer. The C1 peak in the left curve is fitted to the binding energy of C-C and C-O/C=O bonds. All analysis performed by CasaXPS™ software.

The last analysis of surface modification, by ATR-FTIR (Perkins-Elmer, fixed 45 deg incidence, sample in physical contact with Ge crystal), was attempted to confirm the XPS results. Unfortunately, neither large absorptions at specific energies nor significant differences between the variously-modified surfaces were observed (Fig. 4-10), while control Teflon samples showed strong absorption peaks. This could be due to the very thin surface modification layer (close to monolayer) that is below the sensitivity of the instrument/technique.

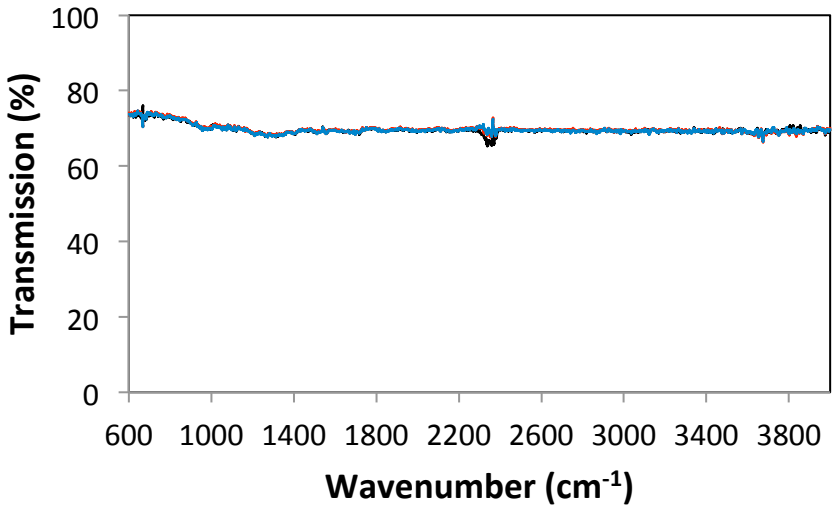


Figure 4-10 Surface analysis with ATR-FTIR. Black, red, and blue lines correspond to the results from pristine bare, APTES-modified, and APTES+GA-modified Si wafers, respectively. No difference was observed among the three conditions.

In summary, we have introduced APTES, APTES+GA, and TBA modification as three methods for antibody protein modification, and successfully demonstrated and confirmed by contact angle measurement and XPS analysis modification of silicon/native oxide wafer, which

has the same surface properties as SiNW. In the next section, I discuss and analyze antibody modification through enzyme-linked immune sorbent assay (ELISA) based on APTES, GA, TBA, and EDC/NHS chemical modification on the SiNW surface to realize a reliable and label-free kinked NWFET biosensor.

4-4. Analysis of antibody modifications on SiNWFET biosensor with ELISA

The Si surface functionalized with aldehyde or amino groups from APTES, APTES+GA, or TBA modification can now bond with antibody proteins. At this point, Enzyme-Linked ImmunoSorbent Assay (ELISA) was employed to investigate both the coupling efficiency of the modified substrate to antibodies and their density at each modification step, as these are significant factors in the effectiveness of the NWFET biosensor. ELISA is a quick and accurate test using secondary antibodies that bind to primary antibodies (PAs) at labeled, verifiable sites. In order to quantitate antibody density on the surface of NW, gold nanoparticle (Au) conjugated secondary antibodies were used to identify the bound sites of antibodies with Au imaging on NW by high-resolution SEM and TEM. In this section, I describe the preparation and modification of Au-conjugated secondary antibody for ELISA and discuss the density of antibody sites as determined by SEM and TEM.

ELISA preparation and application

To calibrate the number of bound antibody sites on 30-nm or 80-nm diameter SiNWs, 5-nm diameter Au-conjugated secondary antibodies (Au-CSA) (Sigma-Aldrich, Anti-Mouse Immunoglobulin-Gold antibody product) were employed. Typical Au-CSA are suspended in

buffer solution with contaminants such as bovine serum albumin (BSA), glycerol, and sodium azide, which are intended to prevent aggregation, freezing and bacterial degradation respectively. However, because these contaminants could interfere with the chemical reactions with the functionalized SiNW surface during antibody modification, dialysis is used to remove them. Ultrafiltration is not used for filtering because the tremendous centrifugal forces (14,000 x g) involved could rupture the link between gold nanoparticle and antibody. Instead, taking into account the molecular weight (MW) of the antibody (immunoglobulin) from Fig. 4-11, a 8-10 kD membrane dialysis kit (Spectrumlabs, Micro Float-A-Lyzer) is used for purification of Au-CSA solution with stirring in a PBS 1X reservoir for ~6 hours. We expect the purified solution to be a mixture of Au-conjugated antibody and BSA in PBS 1X solution due to the similarity of their MW. However, the existence of BSA in ELISA should not disturb the binding event between Au-CSA and the SiNW surface modified by the PAs because BSA is a widely used protein for surface passivation which prevents non-specific binding[54] and ensures the separation of Au-CSA in high ionic strength solution as PBS 1X.

The filtered Au-CSA colloids are directly drop-casted to PA-modified SiNWs for two hours followed by rinsing with DI water and gently blowing dry with nitrogen gas. The final substrate, including Au-CSA/PA complex-modified SiNWs, was moved into SEM or TEM for quantitative analysis of binding density.

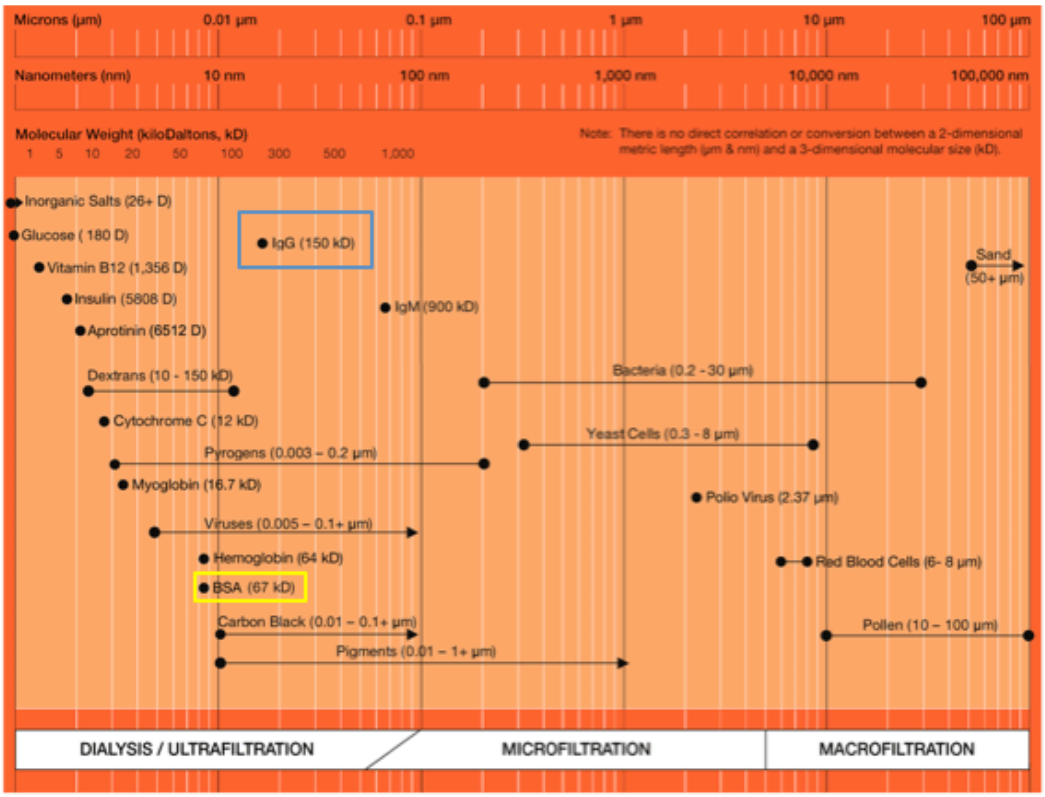


Figure 4-11 Logarithmic pore size chart of molecular weight for nano- and micro- structures. The blue and yellow boxes indicate the sizes of immunoglobulin and BSA respectively. Courtesy of Ref [55].

SEM and TEM analysis of antibody density on the SiNW after surface modification

Scanning Electron Microscopy (SEM) is a powerful tool for investigating material properties at the nanoscale. The interaction between a solid specimen and an irradiated electron can produce secondary electrons (SE), back-scattered electrons (BSE), characteristic X-rays, cathodoluminescence, and transmitted electrons, which contain information about the sample's surface structure (morphology), crystallinity, chemical composition, and orientation of

material.[56] SE imaging is commonly used to achieve high-resolution images of a sample surface up to ~1 nm; however, this mode cannot provide high-resolution contrast for the gold nanoparticles linked to semiconducting nanowire. In contrast, since BSE signal is sensitive to atomic number, the energy selective back-scattering (ESB) detector, which filters out secondary electrons, is used to image 5-nm Au-linked SiNW, and it successfully demonstrates clear contrast between gold nanoparticles and SiNW without loss of nanoscale resolution. Fig. 4-12a-d show typical SEM images in ESB mode of bare SiNW and prostate specific antigen antibody (anti-PSA)-modified SiNW with APTES+GA, TBA, and APTES+NHS/EDC after Au-CSA modification. Due to the significant difference in atomic mass between Si and Au, the images show dark contrast for SiNWs as compared with gold nanoparticles.

Based on multiple SEM (FESEM Ultra Plus, Zeiss) images from different NWs on the sample chip, antibody density on SiNW is determined by counting the number of Au colloids on NWs. The statistical results for different surface modifications are shown in Fig. 4-12e. The area used for density calculation is calibrated from a semi-circular cylinder because all the SEM images are projected ones. All three surface modification methods demonstrated statistically significant distinct protein coupling densities compared to the bare Si control, with APTES+GA>APTES+EDC/NHS>TBA, though all were within the same order of magnitude.

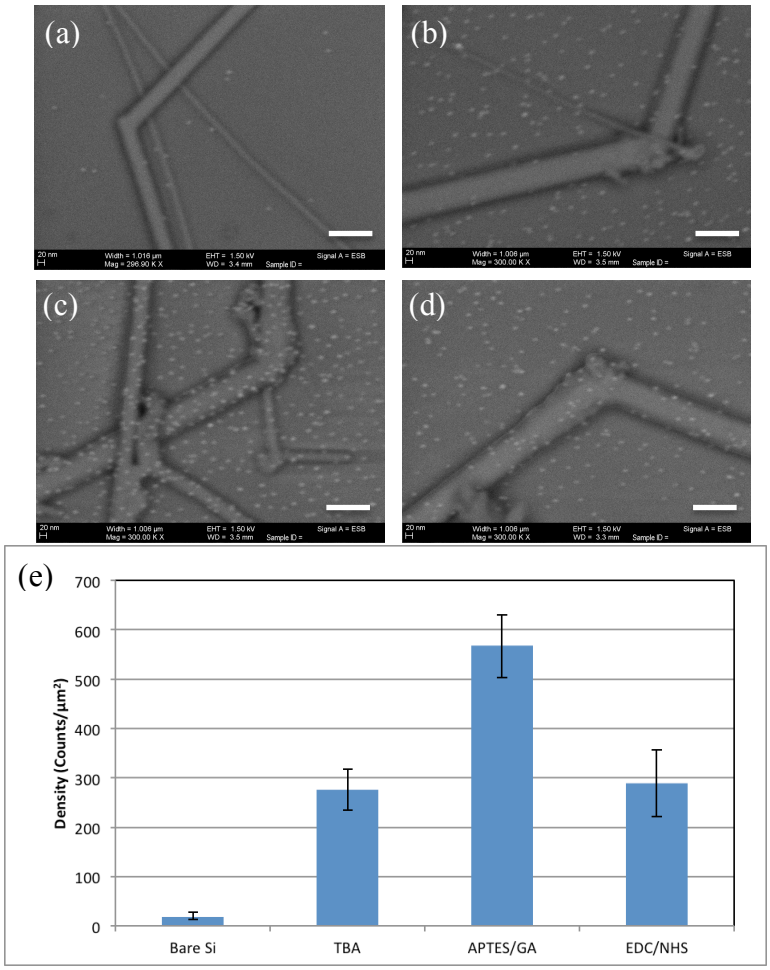


Figure 4-12 Statistical analysis of anti-PSA density on SiNW after surface modifications based on SEM imaging in ESB mode. Note that the position of a gold nanoparticle corresponds to anti-PSA location by specific binding of anti-PSA and secondary antibody. (a), Bare SiNW for control. Scale bar: 100 nm. (b), anti-PSA SiNW modified by TBA. Scale bar: 100 nm. (c), anti-PSA SiNW modified by APTES+GA. Scale bar: 100 nm. (d), anti-PSA SiNW modified by APTES+EDC/NHS. Scale bar: 100 nm. (e), Statistical results of Au density in the cases of (a)-(d), based on SEM images. Each result is averaged from 10 photos of different regions of the sample chip.

For more precise analysis, TEM (Jeol 2100 TEM, Jeol) imaging is performed with the same SiNW samples used in SEM analysis. All surface modifications of NWs are done on silicon nitride membrane (500 μm x 500 μm x 38 nm) for TEM imaging. Fig. 4-14a-d show typical TEM images of Au-CSA modified SiNWs with bare surface (control) and prostate specific antigen antibody (anti-PSA)-modified surfaces with APTES+GA, TBA, and APTES+NHS/EDC. Unlike SEM images, for purposes of the density calculation the total area should include anywhere the 5-nm gold nanoparticle can contact, because TEM can reveal the entire area. Fig. 4-13 indicates that a 5-nm gold nanoparticle can attach in the angle range of 2π-Θ on the surface of the NW, where Θ is $2\arccos\left(\frac{D-5}{D+5}\right)$. Therefore, the effective area is

$$W \cdot L = L \cdot D \cdot \left(\pi - \arccos\left(\frac{D-5}{D+5}\right)\right) \tag{4-16}$$

where L is a nanowire length. Based on this, anti-PSA coupling densities for all surface modification methods were calibrated and statistically analyzed; the results are shown in Fig. 4-14e. As expected and in agreement with SEM analysis, the control (bare Si) shows significantly (15 ~ 50 times) lower density than the others. Strangely, however, the APTES+NHS/EDC modification yields a density ~3 times higher than TBA and even APTES+GA modification, a result that is not in agreement with the SEM data.

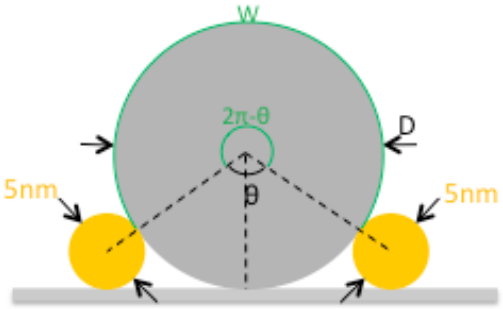


Figure 4-13

Figure 4-13 (Continued)

Figure 4-13 Schematic for calculation of the effective area where 5-nm diameter gold nanoparticles can bind. W and D are the available boundary lines for gold nanoparticles and NW diameter, respectively. A gray circle and two golden circles represent the SiNW and gold nanoparticles, respectively.

Even though there are fluctuations in the ELISA results for anti-PSA density on SiNW depending on analysis methods, both the APTES+GA and APTES+EDC/NHS modifications demonstrate at least ~600 per μm^2 average anti-PSA density. This means that ~27 mV would be induced on the surface of SiNW in PBS 1 mX if antigens capable of ten charges fully occupy all the binding sites, based on the simulation in Section 4.1.

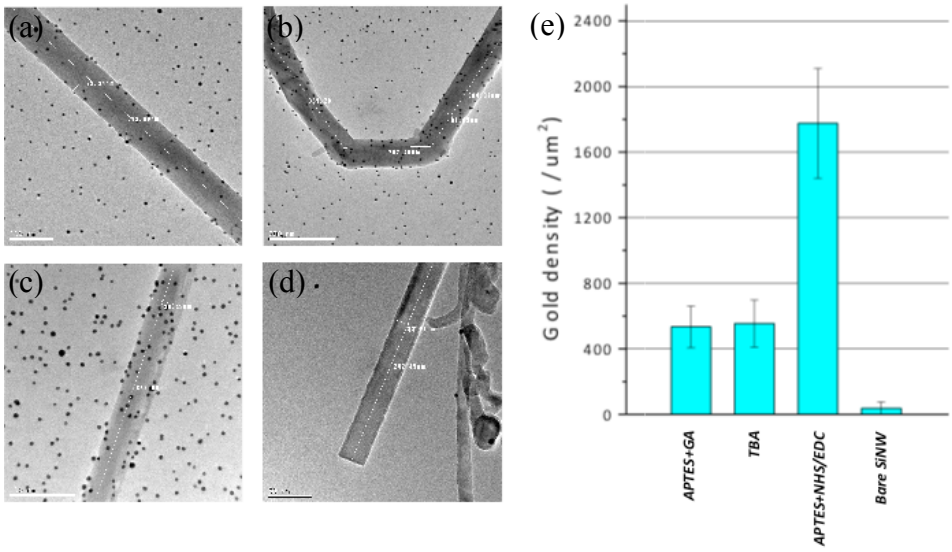


Figure 4-14 Statistical analysis of anti-PSA density on SiNW after surface modifications based on TEM imaging. (a), anti-PSA modified SiNW by APTES+GA. Scale bar: 100 nm. (b), anti-PSA modified SiNW by TBA. Scale bar: 200 nm. (c), anti-PSA modified SiNW by APTES+EDC/NHS. Scale bar: 100 nm.

Figure 4-14 (Continued) (d), Bare SiNW for control. Scale bar: 50 nm. (e), Au density results for (a)-(d) based on TEM images. Each result is averaged from 10 photos of different regions of the sample chip.

4-5. Conclusion

This chapter investigates a novel kinked NWFET biosensor created by bottom-up methods. First, the theoretical simulation in Section 4-1 of a typical NWFET biosensor with an antibody layer on its surface producing an ion-screening effect predicts its high sensitivity in low ionic strength solution. Specifically, the simulation predicts that ~4.8 mV of gate potential change on the device surface could be induced by one hundred binding events of a single charged antigen per μm in 1 μM ionic strength solution. Second, a novel kinked semiconducting nanowire is successfully synthesized by modulation of morphology and dopants for use as a 3D probe-type biosensor. Furthermore, n-type kinked NWFET fabricated from the grown NW is characterized in buffer solution and revealed to have a high sensitivity (i.e. transconductance to noise ratio) capable of detecting five bound single charges. Third, various approaches for surface functionalization on a Si wafer are both qualitatively and quantitatively evaluated by contact angle measurement and XPS analysis. These confirmed well-modified chemical layers of aldehyde and amino groups necessary for covalent bonding with antibodies. Following these functionalizations, the yields of antibody on SiNW after modification processes are statistically investigated by the ELISA method using gold-nanoparticle conjugated secondary antibodies. SEM and TEM images of gold nanoparticles on SiNW reveal an average antibody density of at

least ~600 per μm^2 where the NW surface was functionalized by either APTES+EDC/NHS or APTES+GA.

Based on our understanding of the NWFET biosensor and its surface modification established in this chapter, I will next demonstrate reliable and reproducible detection of charged molecules with a kinked NWFET biosensor using a microfluidic system at low ionic strength solution. In addition, I will introduce the concept of a NW biosensor that can function at high ionic strength, which must underlie our efforts to realize an intracellular biomolecule-sensing NW probe.

Bibliography

1 Lindberg, V. & Hellsing, B. Metallic quantum dots. *J. Phys.: Condens. Matter* **17**, S1075-S1094 (2005).

2 Bányal, L. & Koch, S. W. Semiconductor quantum dots: Series on atomic, molecular and optical physics. (World Scientific, 1993).

3 Schwartz, D. A., Norberg, N. S., Nguyen, Q. P., Parker, J. M. & Gamelin, D. R. Magnetic quantum dots: Synthesis, spectroscopy, and magnetism of Co^{2+}- and Ni^{2+}-doped ZnO nanocrystals. *J. Am. Chem. Soc*. **125**, 13205–13218 (2003).

4 Ajayan, P. M. & Ebbesen, T. W. Large-scale synthesis of carbon nanotubes. *Nature* **358**, 220-222 (1992).

5 Ishai, M. B. & Patolsky, F. Shape- and dimension-controlled single-crystalline silicon and SiGe nanotubes: Toward nanofluidic FET devices. *J. Am. Chem. Soc.* **131**, 3679–3689 (2009).

6 Cui, Y., Lauhon, L. J., Gudiksen, M. S., Wang, J. & Lieber, C. M. Diameter-controlled synthesis of single-crystal silicon nanowires. *Appl. Phys. Lett.* **78**, 2214-2216 (2001).

7 Gudiksen, M. S., Lauhon, L. J., Wang, J., Smith, D. & Lieber, C. M. Growth of nanowire superlattice structures for nanoscale photonics and electronics. *Nature* **415**, 617-620 (2002).

8 Lauhon, L. J., Gudiksen, M. S., Wang, D. & Lieber, C. M. Epitaxial core-shell and core-multi-shell nanowire heterostructures. *Nature* **420**, 57-61 (2002).

9 Yin, A. J., Li, J., Jian, W., Bennett, A. J. & Xu, J. M. Fabrication of highly ordered metallic nanowire arrays by electrodeposition. *Appl. Phys. Lett.* **79**, 1039-1041 (2001).

10 Geim, A. K. & Novoselov, K. S. The rise of graphene. *Nature Mater.* **6**, 183-191 (2007).

11 Sohn, L. L. & Saleh, O. A. An artificial nanopore for molecular sensing. *Nano Lett.* **3**, 37-38 (2003).

12 Jiri, H. *Surface plasmon resonance based sensors.* (Springer, 2006).

13 Maxwell, D. J., Emory, S. R. & Nie, S. Nanostructured thin-film materials with surface-enhanced optical properties. *Chem. Mater.* **13**, 1082–1088 (2001).

14 Kurkina, T. & Balasubramanian, K. Towards in vitro molecular diagnostics using nanostructures. *Cell. Mol. Life Sci.* **69**, 373–388 (2012).

15 Tian, B., Cohen-Karni, T., Qing, Q., Duan, X., Xie, P., & Lieber, C. M. Three-dimensional, flexible nanoscale field-effect transistors as localized bioprobes. *Science* **329**, 831-834 (2010).

16 Duan, X., Gao, R., Xie, P., Cohen-Karni, T., Qing, Q., Choe, H., Tian, B., Jiang, X. & Lieber, C. M. Intracellular recordings of action potentials by an extracellular nanoscale field-effect transistor. *Nature Nanotechnol*. **7**, 174-179 (2012).

17 Gao, R., Strehle S., Tian, B., Cohen-Karni, T., Xie, P., Duan, X., Qing, Q. & Lieber, C. M. Outside looking in: Nanotube transistor intracellular sensors. *Nano Lett.* **12**, 3329-3333 (2012).

18 Rosi, N. L. & Mirkin, C. A. Nanostructures in biodiagnostics. *Chem. Rev*. **105**, 1547−1562 (2005).

19 Gao, Z. & Roy, S. Nanostructure-based electrical biosensors. *Nano Today* **4**, 318-334 (2009).

20 Kerman, K., Endo, T., Tsukamoto, M., Chikae, M., Takamura, Y. & Tamiya, E. Quantum dot–based immunosensor for the detection of prostate-specific antigen using fluorescence microscopy. *Talanta* **71**, 1494-1499 (2007).

21 Cao, Y. C., Jin, R. & Mirkin, C. A. Nanoparticles with Raman spectroscopic fingerprints for DNA and RNA detection. *Science* **297**, 1536-1540 (2002).

22 Grubisha, D. S., Lipert, R. J., Park, H. Y., Driskell, J. & Porter, M. D. Femtomolar detection of prostate-specific antigen: an immunoassay based on surface-enhanced Raman scattering and immunogold labels. *Anal. Chem.* **75**, 5936–5943 (2003).

23 Cui, Y., Ren, B., Yao, J. L., Gu, R. A. & Tian, Z. Q. Multianalyte immunoassay based on surface-enhanced Raman spectroscopy. *J. Raman. Spectrosc.* **38**, 896–902 (2007)

24 Giuffreda, M. G., Negri, F. & Orlandi, G. Quantum-Chemical modeling and analysis of the vibrational structure in the phosphorescence spectrum of C_{60}. *J. Phys. Chem. A*, **105**, 9123–9129 (2001).

25 Janshoff, A., Galla, H. & Steinem, C. Piezoelectric mass-sensing devices as biosensors – An alternative to optical biosensors? *Angew. Chem. Int. Ed.* **39**, 4004-4032 (2000).

26 Minunni, M., Mascini, M. & Gullbault, G. G. The quartz crystal microbalance as biosensor. A status report on its future. *Anal. Lett.* **28**, 749-764 (1995).

27 Patolsky, F., Zheng, G., Hayden, O., Lakadamyali, M., Zhuang, X. & Lieber, C. M. Electrical detection of single viruses. *Proc. Natl. Acad. Sci. USA* **101**, 14017-14022 (2004).

28 Zheng, G., Patolsky, F., Cui, Y., Wang, W. U. & Lieber, C. M. Multiplexed electrical detection of cancer markers with nanowire sensor arrays. *Nature Biotechnol.* **23**, 1294-1301 (2005).

29 Andreescua, S., Barthelmebsa, L. & Marty, J. Immobilization of acetylcholinesterase on screen-printed electrodes: comparative study between three immobilization methods and applications to the detection of organophosphorus insecticides. *Anal. Chim. Acta.* **464**, 171-180 (2002).

30 Patolsky, F., Zheng, G. & Lieber, C. M. Nanowire-based biosensors. *Anal. Chem.* **78**, 4260–4269 (2006).

31 Stern, E., Wagner, R., Sigworth, F. J., Breaker, R., Fahmy, T. M. & Reed, M. A. Importance of the Debye screening length on nanowire field effect transistor sensors. *Nano Lett.* **7**, 3405–3409 (2007).

32 Tian, B., Xie, P., Kempa, T. J., Bell, D. C. & Lieber, C. M. Single crystalline kinked semiconductor nanowire superstructures. *Nature Nanotechnol*. **4**, 824-829 (2009).

33 Duan, X. & Lieber, C. M. General synthesis of compound semiconductor nanowires. *Adv. Mater.* **12**, 298-302 (2000).

34 Xiang, J., Lu, W., Hu, Y., Wu, Y., Yan, H. & Lieber, C. M. Ge/Si nanowire heterostructures as high-performance field-effect transistors. *Nature* **441**, 489-493 (2006).

35 Jiang, X., Xiong, Q., Nam, S., Qian, F., Li, Y. & Lieber, C. M. InAs/InP radial nanowire heterostructures as high electron mobility devices. *Nano Lett*. **7**, 3214-3218 (2007).

36 Wu, Y., Cui, Y., Huynh, L., Barrelet, C. J., Bell, D. C. & Lieber, C. M. Controlled growth and structures of molecular-scale silicon nanowires. *Nano Lett.* **4**, 433-436 (2004).

37 Sze, S. M. *Semiconductor Device – Physics and Technology* (John Wiley & Sons, 2002).

38 Gao, X. P., Zheng, G. & Lieber, C. M. Subthreshold regime has the optimal sensitivity for nanowire FET biosensors. *Nano Lett.* **10**, 547-552 (2010).

39 Reitz, J. R., Milford, F. J., Christy, R. W. *Foundation of Electromagnetic Theory.* (Addison-Wesley, 2008).

40 Russel, W. B., Saville, D. A. & Schowalter, W. R. *Colloidal Dispersions.* (Cambridge University Press, 1989).

41 Sommerfeld, A. *Partial Differential Equations in Physics.* (Academic Press, 1949).

42 Levine, I. N. *Physical Chemistry*. (McGraw-Hill, 2009).

43 Jiang, Z., Qing, Q., Xie, P., Gao, R. & Lieber, C. M. Kinked p-n junction nanowire probes for high spatial resolution sensing and intracellular recording. *Nano Lett.* **12**, 1711-1716 (2012).

44 Li, Y., Qian, F., Xiang, J. & Lieber, C. M. Nanowire electronic and optoelectronic devices. *Mater. Today* **9**, 18-27 (2006).

45 Schematic of a kinked-nanowire nanoFET sensor probing the interior of a cell. http://cmliris.harvard.edu/research/image-gallery/

46 Edington, J. W. *Practical electron microscopy in materials science, 2. Electron diffraction in the electron microscope.* (Philips technical library, 1975).

47 Mclachlan, A. D. Protein structure and function. *Annu. Rev. Phys. Chem.* **23**, 165-192 (1972).

48 Carey, F. A. *Organic Chemistry*. (McGraw-Hill Companies, 2000).

49 Janssen, D., Palma, R. D., Verlaak, S., Heremans, P. & Dehaen, W. Static solvent contact angle measurements, surface free energy and wettability determination of various self-assembled monolayers on silicon dioxide. *Thin Solid Films* **515**, 1433-1438 (2006).

50 Briggs, D. & Seah, M. P. *Practical surface analysis by Auger and X-ray photoelectron spectroscopy.* (John Wiley & Sons, 1983)

51 Iwamoto, R. & Ohta, K. Quantitative surface analysis by Fourier transform attenuated total reflection infrared spectroscopy. *Appl. Spectrosc*. **38**, 359-365 (1984).

52 Zeng, X., Xu, G., Gao, Y. & An, Y. Surface wettability of (3-Aminopropyl) triethoxysilane self-assembled monolayers. *J. Phys. Chem. B* **115**, 450–454 (2011).

53 Tuong, S. D., Lee, H. & Kim, H. Chemical fixation of polyelectrolyte multilayers on polymer substrates. *Macromol. Res.* **16**, 373-378 (2008).

54 Sweryda-Krawiec, B., Devaraj, H., Jacob, G. & Hickman, J. J. A new interpretation of serum albumin surface passivation. *Langmuir* **20**, 2054-2056 (2004).

55 *Pore size chart*. http://www.spectrumlabs.com/dialysis/PoreSize.html

56 Goldstein, J., Newbury, D. E., Joy, D. C., Lyman, C. E., Echlin, P., Lifshin, E., Sawyer, L. & Michael, J. R. *Scanning Electron Microscopy and X-ray Microanalysis.* (Springer, 2003).

Chapter 5

A novel kinked nanowire biosensor and opportunities for biomolecular detection under physiological conditions

The advent of the NWFET biosensor in the early 2000s met growing demands for a highly sensitive, label-free and real-time biosensor capable of multiplexed detection.[1-3] Nonetheless, most people in molecular diagnostics and biology still prefer optical biosensors based on fluorescence or surface plasmons to an electrochemical biosensor,[4, 5] due to two issues that are critical in biological and physiological research. The first concerns a fundamental limitation of biosensors based on an electrochemical transduction: ions in solution can surround the charged analytes and screen their potential so that an electrochemical biosensor based on charge sensing loses the power to detect analytes that are a distance greater than the Debye length from the device. At physiological ionic strengths, the Debye length is ~0.7 nm, so that the biosensor essentially becomes blind under these conditions.[6] The second is that a typical NWFET biosensor attached to a substrate, when fabricated by top-down methods, does not allow intracellular detection owing to structural limitation. Expanding the sensing ability of the high-performance biosensor from *in vitro* to *in vivo* is essential for its practical implementation in real-time pathology and, in future, proteomics.

Kinked NWFETs, synthesized by controllable modulation of growth direction and dopant, represent a promising platform to overcome these shortcomings. They feature a probe-like structure in addition to the biosensing advantages of the NWFET.[7-9] In this chapter, I discuss novel kinked NWFET biosensors for intracellular detection. First of all, based on optimized surface modification as discussed in Chapter 4, reliable detection of cancer markers will be demonstrated by n-type kinked NWFET in low ionic strength solution using microfluidics. Furthermore, the concept of a high-frequency-based NWFET biosensor will be introduced, along with a frequency mixing technique for biosensing at high ionic strength.

5-1. Biosensing measurement system with microfluidics

Microfluidics involves the manipulation and delivery of fluids in a precise and controllable manner, which is key to managing biomedical samples reliably and reproducibly. Specifically, compared to a droplet delivery system, microfluidics allows higher throughput, in-situ monitoring, and laminar supplementing of samples. To investigate the behavior of the kinked NWFET biosensor unambiguously this precise control[10] is invaluable. In addition to benefiting from the accuracy conferred by microfluidics, all electrical measurements in low ionic strength biosensing experiments are performed with low-frequency alternating current (AC) modulation, filtering out background noises. In this section, I describe how to set up a conventional electrical measurement system with AC modulation as well as a microfluidic system for biosensing of cancer markers.

Microfluidics

Fig. 5-1 shows the typical pattern of a microfluidic channel designed on a photomask. The pattern is composed of 1.5-mm diameter circles for an inlet and an outlet and 5 mm (length) x 0.5 mm (width) dimension for the main channel. This design (especially the 0.5 mm width) enables laminar delivery of biomolecules.[11] To create a master mold, the photomask was used with a film of SU-8 3050 which was spin-coated at 3000 rpm for 40 s and prebaked at 95^{o}C for 15 min. It should be noted that the spin-coating conditions were designed to form a ~50-μm microfluidic chamber height (10:1 width-to-height aspect ratio) to prevent blockage of the main channel by deflection/deformation of the ceiling during liquid pumping.[12] The pattern for a master mold is then ready following baking at 95^{o}C for 5min and developing with SU-8 developer. For fabrication of the microfluidic chamber with the master mold, soft polymer polydimethylsiloxane (PDMS) is used with a curing agent (Sylgard 184, Dow Corning). A 10:1 (w/w) mixture of PDMS and the curing agent is poured into a petri dish with the master mold to a depth of ~1.5 mm, followed by removal of bubbles under vacuum. The petri dish is then hard-baked in an oven at 80^{o}C for 2 hours to cure the PDMS. Having peeled the cut-out PDMS chamber from the Si wafer with a sharp razor blade, inlet and outlet holes were made by a puncher (Harris Uni-Core^{TM}, Ted Pella, Inc.) followed by cleaning via sonication in acetone for 5 min and in IPA for 5 min.

The PDMS chamber can be installed on the device chip with an optical microscope and an xyz translation stage in a precise manner. Fig. 5-1b and c show our typical microfluidic chamber installed on the region of kinked NWFET devices with precise alignment. After alignment, the chamber is sealed by physical pressure with a cover from above and biocompatible silica glue (KWIK-SIL, World Precision Instruments). Note that conventional

sealing with the permanent bond of PDMS[13] cannot be used for our microfluidic set-up due to surface functionalization of the substrate.

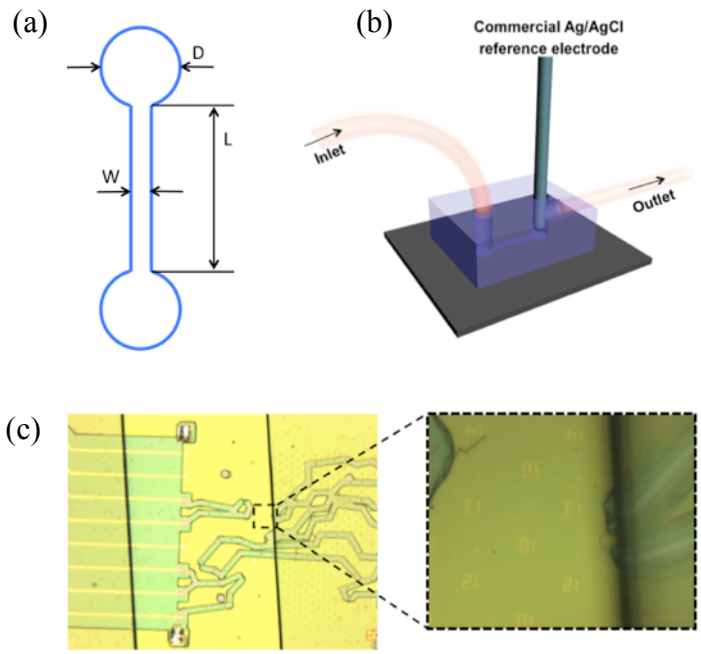


Figure 5-1 Microfluidics. (a), Design of microfluidic channel. D, W, and L correspond to 1.5 mm, 500 μm, and 5 mm respectively. (b), Schematic of microfluidic chamber on chip. Note that the Ag/AgCl reference electrode is inserted at the outlet to maintain stable solution potential. (c) PDMS chamber installed on the device chip with accurate alignment. Aligned PDMS channel allows exposure of only the nanowire to solution (right).

In order to dispense the biomolecule solution manageably and minimize artifacts, we used a syringe pump (Standard Infuse/Withdraw Harvard 33 Twin Syringe Pumps, Harvard

Apparatus) at the end of the outlet and a rotary switch valve (Automated 6-position 7-port low pressure selector valve, Rheodyne) in the middle of the inlet tube as shown Fig. 5-2. Electrical signals during biosensing experiments can be induced not only by molecular binding/unbinding events but also by some artifacts as explained in the Appendix (e.g. change of ionic strength or pH, static charge disturbance from physical contact). Use of the rotary switch valve prevents cross-contamination of solutions and minimizes external interference during the change of reservoirs.

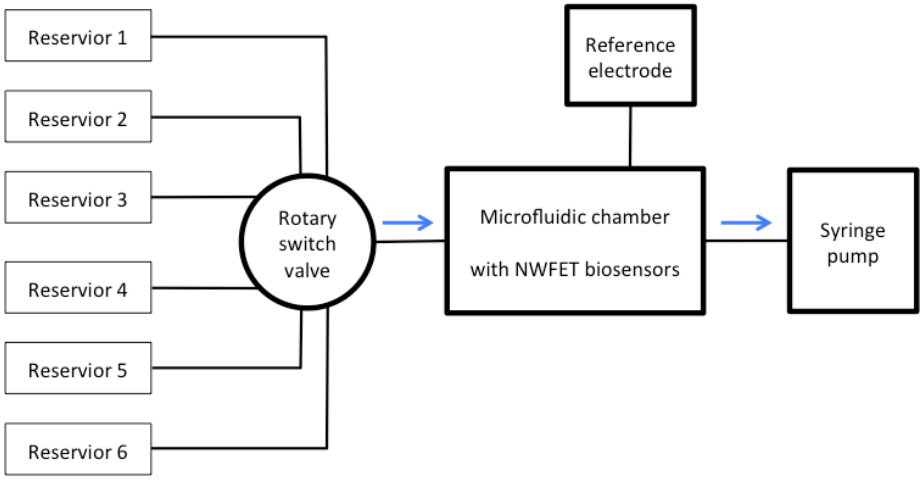


Figure 5-2 Block diagram of the microfluidic system for biosensing. Rotary switch valve and syringe pump allow minimal disturbance of the system and flow control, respectively. Blue arrow indicates direction of solution flow.

Set-up for electrical measurement

The electrical set-up is composed of a function generator and a Lock-in amplifier (SR830 Lock-in, Stanford Research Systems) for an electrical measurement through amplitude modulation. AC voltage at low frequency and DC voltage are applied to the NWFET biosensor by a function generator for V_{sd} and solution for a water-gate V_{WG} through reference electrode, respectively. The AC signal modulated by the gate potential change of NWFET can be monitored by the Lock-in which filters noise in the output. The Lock-in enables removal of different frequency signals from the input by a homodyne detection mechanism with low pass filter,[14] making it possible to monitor the NWFET signal with low noise. Fig 5-3 shows a noise level in DC (without a Lock-in) and AC (with a Lock-in) measurement for the same NWFET. The AC measurement with a Lock-in yielded an order of magnitude less noise than the DC measurement.

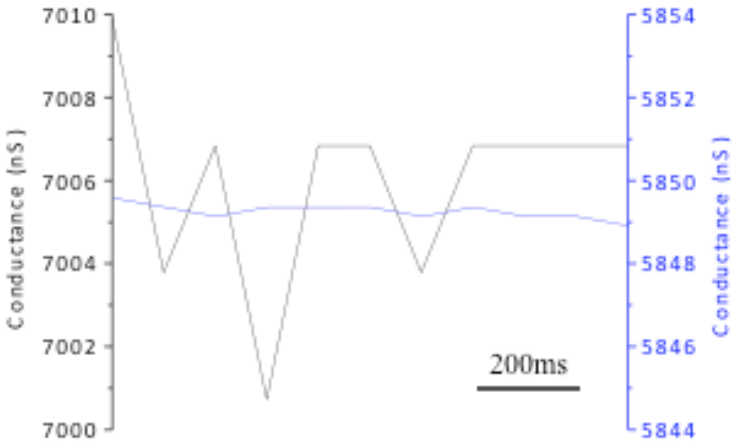


Figure 5-3 Noise levels for DC and AC (with Lock-in amplifier) measurements. Conductance of the same device was monitored with either DC (black) or AC (blue) measurement. For DC, a 10-kHz low-pass filter was used before the Analog-to-Digital converter. For AC, the time constant was set at 100 ms in the Lock-in amplifier.

So far I have described the development of the microfluidic system and AC electronic set-up designed to achieve high signal-to-noise for the realization of reliable and reproducible biosensing. In the next section, using this system, I will describe the electrical sensing of cancer markers with an n-type kinked NWFET biosensor in low ionic strength solution and compare the empirical data with the theoretical predictions discussed in Chapter 4.1.

5-2. Biomolecular detection with a kinked NWFET biosensor in low ionic strength solution

The NWFET biosensor can detect not only the binding/unbinding of charged target biomolecules but also other factors that affect the gate potential of the device. These artifacts can make it difficult to analyze the data collected from the biosensor clearly. Therefore, we used ELISA methods with 5-nm gold nanoparticle conjugated secondary antibodies (Au-CSA), which allows investigation of surface functionalization and antibody modification, to demonstrate a kinked NWFET biosensor due to several advantages. First, Au-CSA specifically binds with only primary anti-PSA on the surface of the device, enabling confirmation of device selectivity. Second, an association and dissociation of Au-CSA can be detected electrochemically because both gold nanoparticles linked to the antibody and the antibody itself are electrically charged in solutions of specified pH. The isoelectric points (pIs) of gold nanoparticle and immunoglobulin are known to be ~3[15] and 6.1~ 8.5[16]. More significantly, gold nanoparticles linked to secondary antibodies can be imaged by SEM in Energy Selective Backscattering (ESB) detection mode after electrical sensing of Au-CSA is completed, so that the source of electrical signal change can be confirmed.

Au-CSA sensing experiments in low ionic strength solution were performed with p-type straight NWFETs (the control) and n-type kinked NWFETs in the microfluidics system. All NWFETs were functionalized by APTES+GA followed by anti-PSA modification, and simultaneously monitored through 79 Hz measurement with Lock-in. Fig. 5-4 shows the results, which demonstrate the conductance changes of complementary NWFETs after introducing and rinsing Au-CSA in PBS 1 mX (pH 6.0). Several observations can be made. First, the direction of conductance changes, an increase (decrease) for p-type NWFETs and a decrease (increase) for n-type NWFETs, due to the association (dissociation) of negative charges on their surfaces, are in accordance with the theoretical expectation of charge polarity for Au-CSA at pH 6. Second, two different n-type kinked NWFETs exposed to the same microfluidic conditions had generally similar conductance profiles, differing only in some details of the signal (Fig. 5-4d). These observations are evidence that the conductance changes are caused by Au-CSA binding/unbinding on individual NWFET biosensors. Third, the conductance of the biosensors after the rinsing process did not fully return to the baseline before Au-CSAs introduction. The observed baseline shifts are -24 mV, -28 mV, and +36 mV for device L17-L20 (Fig. 5-4a), device L18-L19 (Fig. 5-4b), and device L9-L10 (Fig. 5-4c), respectively. These values should correspond to induced gate potential changes of the devices by undissociated Au-CSAs, if the electrical signal reflects the binding/unbinding events of biomolecules on the surface of the device. Note that the gate potential changes are calibrated from the transconductance of the devices in PBS 1 mX.

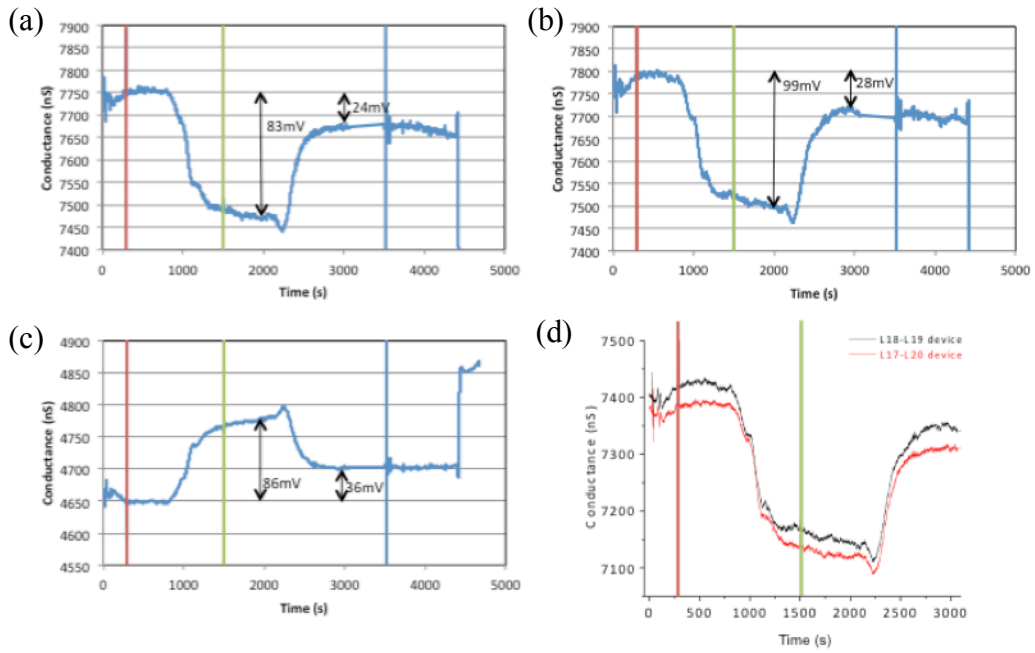


Figure 5-4 Au-CSA sensing results. Red and green lines indicate when flow of 100 nM Au-CSA colloid in PBS 1 mX and PBS 1 mX alone begins, respectively. The blue line in (a)-(c) indicates the starting time for air flow to dry surface. The abrupt signal change around 4500 s corresponds to the time when air arrives at the NWFET devices and all devices are monitored simultaneously. (a), Device L17-L20 (n-type kinked NWFET), (b) Device L18-L19 (n-type kinked NWFET). (c), Device L9-L10 (p-type straight NWFET). (d), Conductance vs. time curves of two simultaneously monitored devices.

In order to clarify the reason for the shift in baseline conductance, SEM images were taken in ESB mode. Fig. 5.5 shows typical SEM images of a NWFET including the intrinsic semiconductor part. The average Au density from electrically-monitored NWFETs was ~123/μm^2 which is similar to the Au density from the Si_3N_4 substrates. Because the baseline of the signal was stable during drying, as shown in Fig. 5-4a-c, we conclude that the remaining Au-

CSAs along the NWFET channel induced the baseline shifts for the three devices. Therefore, based on these data, we can calculate induced gate potential by a single Au-CSA binding event in a 1-μm^2 area of the nanowire as well as the Au density for devices L17-L20, L18-L19, and L9-L10 in which all binding sites for Au-CSAs are occupied, as shown in Table 5-1. If we use the gate potential change on a NWFET by a single charged protein from theoretical simulation in Chapter 4.1, these experimental results reveal that a single Au-CSA carries ~4 charges in pH 6 PBS 1 mX.

Table 5-1 Summary of results for Fig. 5-4a-c

	Device L17-L20 (n-type)	Device L18-L19 (n-type)	Device L9-L10 (p-type)
Gate potential change by a single Au-CSA in 1 μm^2	$\frac{-24mV}{123} = -0.20mV$	$\frac{-28mV}{123} = 0.23mV$	$\frac{+36mV}{123} = 0.29mV$
Au density in equilibrium after Au-CSA introduction	$\frac{-83mV}{-24mV} \times \frac{123}{\mu m^2} = 425/\mu m^2$	$\frac{-99mV}{-28mV} \times \frac{123}{\mu m^2} = 435/\mu m^2$	$\frac{86mV}{36mV} \times \frac{123}{\mu m^2} = 294/\mu m^2$

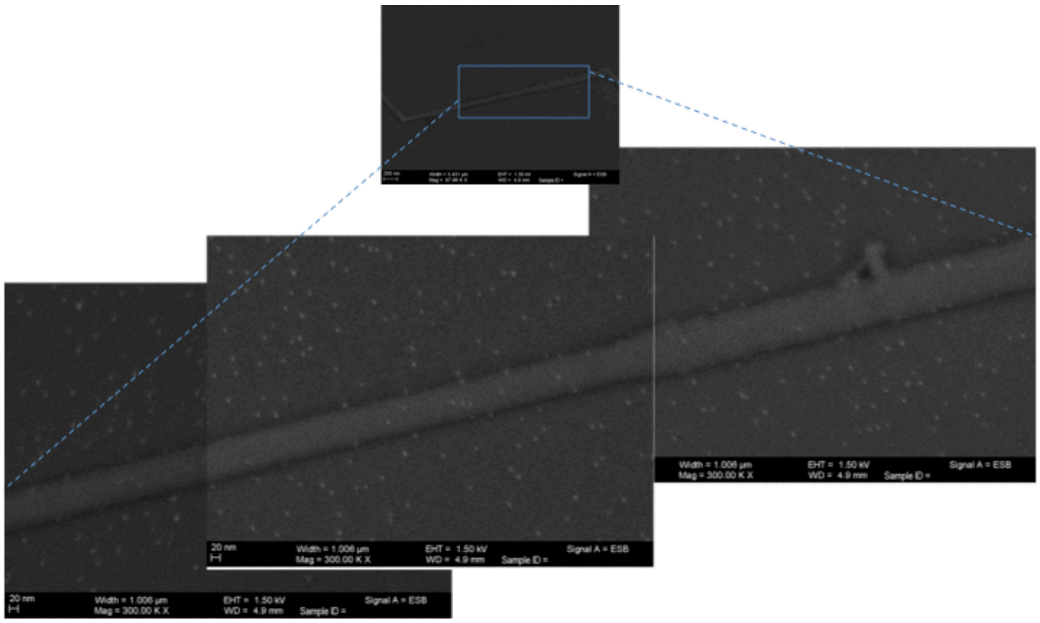


Figure 5-5

Figure 5-5 (Continued)

Figure 5-5 Typical SEM images of NWFET biosensor in ESB mode after the Au-CSA sensing experiment. Three high-resolution SEM images are joined to more accurately quantify the attached Au in the area outlined by the blue box.

Subsequently, the capacity of the kinked NWFET for sensing charged biomolecules was clearly verified by the ELISA method with Au-CSA. In addition, the number of carried charges in a single gold-nanoparticle linked to a cancer marker was successfully calibrated in low ionic strength solution by comparison of the theoretical simulation and empirical results. In the next section, I will discuss a new approach for a biomolecular sensor with NWFET in high ionic strength solution with the aim of envisioning a novel 3D biomolecular sensing probe capable of functioning at physiological solution concentrations.

5-3. Toward biomolecular detection at high ionic strength

As mentioned in the introduction to this chapter, one of the biggest challenges in expanding implementation of the nanowire electrochemical biosensor into point-of care or *in vivo* investigations is overcoming the ion-screening effect caused by a short Debye length[17] in high ionic strength medium[18]. Because the Debye length in a physiological environment is less than 0.7 nm, the conventional NWFET biosensor cannot detect the existence of target molecules on its surface due to the thickness of surface modification layers as well as the actual physical size of the antibody or receptor. In this section, I discuss the NWFET biosensor in high ionic

strength solution, and theoretically propose a novel high-frequency measurement system with a frequency mixer based on impedance change sensing.

Before discussing a potential solution we need first of all to understand the NWFET biosensor at high ionic strength. The system of an antibody-modified NWFET in solution is composed of the reference electrode, medium, an interface between the medium and a surface modification layer, and a gate oxide and semiconductor nanowire channel. Fig. 5-6a depicts this system before and after the association of target antigens with the antibody layer. Assuming that the antibody layer forms a membrane by close packing and that all binding sites are occupied by antigens, antigen binding events will give rise to a change in not only resistance but also capacitance between the reference electrode and the NWFET. The important change during antigen binding/unbinding events is the change in capacitance which is not screened by background ions in the solution.

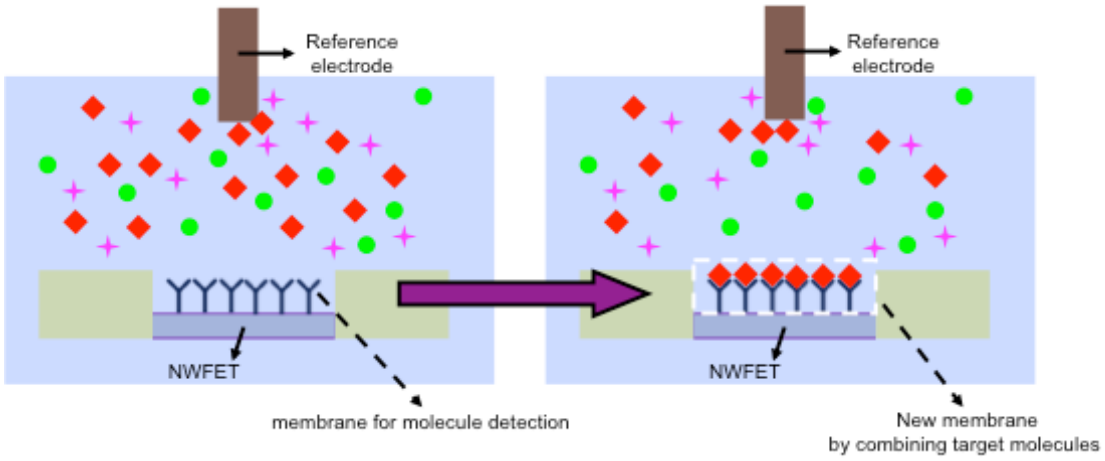


Figure 5-6 Schematic of NWFET biosensor in electrolyte before (left) and after (right) target antigen binding. The purple line on the NWFET, 'Y' shape, red diamond, green circle, and pink cross indicate native gate oxide, antibody, antigen, arbitrary biomolecule, and ions in solution, respectively.

To analyze the system qualitatively, equivalent circuits for Fig. 5-6b are considered. When DC or AC potential are applied to the electrolyte, solvated counter ions create an electrical double layer (EDL) by aligning along the antibody layer, so that this structure can be described as a RC parallel circuit consisting of the capacitance of electrical double layer (C_{DL}), Warburg resistance (W), and charge-transfer resistance (R_{CT})[19]. When electron transfer due to the external electric field starts, the Warburg impedance (W) owing to the mass transport plays a role in determining the surface kinetics at the electrolyte/antibody layer interface. The charge-transfer resistance (R_{CT}), which is the polarization resistance at equilibrium potential, is mainly due to electrochemical kinetics (redox processes) at the interface. Hence, the R_{ct} reflects how dense the functional groups and antibodies are, and will be affected by the number of antibody-antigen complexes and antigens in the electrolyte. C_{DL} is determined by the dipoles at the interface, while W and R_{CT} stem from ion diffusion (non-faradaic) and electrochemical reactions on the surface (faradaic) respectively. Thus the system is composed of three main impedances including the electrical double layer (EDL), the antibody-antigen membrane, and the gate oxide where it will divide an electrical potential applied to the reference electrode. Therefore, a gate bias of high frequency, which will make the impedance of antibody membrane and antibody-antigen complex membrane dominant in the system, would allow significant change of the gate potential right on the gate oxide due to formation and dissolution of the antigen layer.

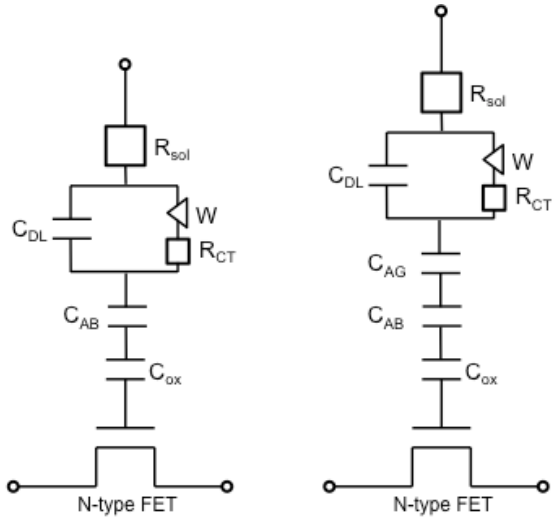


Figure 5-7 Equivalent circuits of n-type NWFET biosensor before (left) and after (right) target antigens. The antibody and antigen layers can be considered a capacitor assuming that they form membranes by close packing.

For clearer analysis, specific parameters of the system are examined and calculated in Table 5-2. Interestingly, the antibody layer is approximately three orders of magnitude smaller than general EDL capacitance and similar to the capacitance of the gate oxide. The impedance of a capacitor is inversely proportional to the capacitance. Therefore, if we assume the impedance of antibody layer is critically larger than that of the EDL without faradaic current at the electrolyte/antibody membrane interface (namely, ignoring W and R_{CT} for simplicity), forming an antigen layer on the antibody layer will induce a significant potential drop and change the current of the NWFET at high frequency gate potential. Furthermore, R_{CT} and W will contribute to changing the NWFET current with high-frequency modulation of gate bias because redox kinetics will be changed by antigen binding and W will be ignorable at high frequency as shown in Table 5-2.

Table 5-2 Specific values of each component in Fig. 5-7

1 μm channel length, 30 nm diameter NWFET	**Values**
Solution conductivity in 0.1 M PBS 1X	~ 1.5 S/m[20]
Electrical double layer capacitance in 0.1 M ionic strength (Stern layer capacitance)	~10^{-12} F (simulated results)[21]
Charge transfer resistance in 0.1 M ionic strength	~3 x 10^5 Ω [22]
Warburg impedance (W)	$\frac{\sqrt{2}\sigma}{\sqrt{2\pi f}}$ $(\sigma : Warburg\ constant)$[23]
Capacitance per unit length of native SiO_2 (1 nm thick)	$\frac{2\pi\varepsilon_0\varepsilon_{SiO_2}}{\ln\left(\frac{31nm}{30nm}\right)}\times 1\mu m = 6.6\times10^{-15}F$
Capacitance per unit length of antibody (10 nm thick) layer	$\frac{2\pi\varepsilon_0\varepsilon_{protein}}{\ln\left(\frac{41nm}{31nm}\right)}\times 1\mu m = 8.0\times10^{-16}F$[24]
Capacitance per unit length of antigen (10 nm thick) layer on antibody (10 nm thick) layer	$\frac{2\pi\varepsilon_0\varepsilon_{SiO_2}}{\ln\left(\frac{51nm}{41nm}\right)}\times 1\mu m = 1.0\times10^{-15}F$[24]

To estimate the NWFET current, we start with the linear regime of NWFET:

$$I_{DS} = \frac{1}{L^2}\mu C_{ox}\left((V_G - V_T)V_{DS}\right) \tag{1-6}$$

The main information we want to focus on for sensing is $\frac{\Delta G}{G}$ where ΔG and G are the conductance change by antigen binding and the initial conductance of NWFET before binding. Here, V_G, the voltage right on the gate oxide, is related to the applied voltage at reference electrode V_R via the complex valued transfer function H(iω), so that

$$V_G = H(i\omega) \times V_R \tag{5-1}$$

H (iω) can be determined by the voltage divider equation neglecting R_{sol} in Fig. 5-7:

$$H(i\omega) = \frac{1 + i\omega RC}{1 + i\omega R(C + C_{ox)}} \tag{5-2}$$

where all the layers from the EDL to the antibody layer (or antibody-antigen complex layer) are considered to form a RC circuit with 'R' and 'C' parameter. Substituting eq. 5-2 into eq. 1-6 and applying $V_G = Asin[(\omega + \Delta\omega)t]$ and $V_{DS} = Asin[\omega t]$,

$$I_{DS} = \frac{1}{L^2}\mu C_{ox}\left(\left(\frac{AH(i\omega)sin[(\omega + \Delta\omega)t](1 + i\omega RC)}{1 + i\omega R(C + C_{ox)}} - V_T\right)Asin[\omega t]\right) \tag{5-3}$$

where A is constant. Once a B cos[Δωt] generated by a frequency mixer and low pass filter (after using trig identities) is applied to the Lock-in for the reference, only the cos[Δωt] term in $H(i\omega)V_R V_{DS}$ will be measured. Now, let $H(i\omega) = He^{i\phi}$, where H and ϕ are the magnitude and the phase of the transfer function respectively. Then, eq. 5-1 becomes

$$\begin{aligned} V_G &= H(i\omega)\times Asin[(\omega + \Delta\omega)t] = \mathrm{Im}\left[\mathrm{A}He^{i(\omega+\Delta\omega)t+\phi}\right] \\ &= AH\ sin[(\omega + \Delta\omega)t + \phi] \end{aligned} \tag{5-4}$$

Note that, based on the definition of the transfer function in Euler's formula, the antibody-antigen layer will change not only the amplitude (AH) but also cause a phase shift (ϕ). Therefore, eq. (5-3) is

$$I_{DS} = \frac{1}{L^2}\mu C_{ox}\left((AHsin[(\omega + \Delta\omega)t + \phi] - V_T)Asin[\omega t]\right) \tag{5-5}$$

Here, the reference of Lock-in is cos[Δωt] so that the I_{DS} measured by Lock-in is

$$I_{DS} \propto \frac{1}{L^2}\mu C_{ox}A^2 Hsin[(\omega + \Delta\omega)t + \phi]sin[\omega t] \tag{5-6}$$

From trigonometric identity:

$$I_{DS} \propto \frac{1}{L^2}\mu C_{ox}A^2H(sin[(\omega+\Delta\omega)t]\cos[\phi] + \cos[(\omega+\Delta\omega)\,\mathrm{t}]\,sin[\phi])\sin[\omega t] \tag{5-7}$$

Only the first term is in phase with the Lock-in reference. Therefore,

$$I_{DS} \propto \frac{1}{2L^2}\mu C_{ox}A^2H\cos[\phi]\cos[\Delta\omega t] = \frac{1}{2L^2}\mu C_{ox}A^2Re[H(i\omega)]\cos[\Delta\omega t] \tag{5-8}$$

This results show that the measured signal from the Lock-in is proportional to the real part of the transfer function. From eq. 5-2,

$$Re[H(i\omega)] = \frac{1+\omega^2R^2C(C+C_{ox})}{1+\omega^2R^2(C+C_{ox})} = h(\omega,R,C,C_{ox}) \tag{5-9}$$

$$\frac{\partial h}{\partial C} = \frac{C_{ox}\omega^2R^2(\omega^2R^2(C+C_{ox})^2-1)}{(1+\omega^2R^2(C+C_{ox})^2)^2} \tag{5-10}$$

Here, when $\omega R(C+C_{ox}) = 1$, $\frac{\partial h}{\partial C} = 0$ which is an inflection point. Physically, antigen binding should reduce C by the increased thickness, so that positive signals would be observed for $\omega R(C+C_{ox}) < 1$. It is worth noting that there is no term regarding charge here, only a decrease in C. This equation predicts that if ω increases, the sign of the signal will be reversed, when $\omega R(C + C_{ox}) > 1$.

The antigen binding will induce a change in the transfer function so that

$$\frac{\Delta G}{G} = \frac{\Delta h}{h} = \frac{h(\omega,R,C+C_{AB},C_{ox}) - h(\omega,R,C,C_{ox})}{h(\omega,R,C,C_{ox})} \tag{5-11}$$

Here, if C is changed into aC, where $0<a<1$, then

$$S(\omega,R,a,C,C_{ox}) = \frac{\Delta h}{h} = \frac{h(\omega,R,aC,C_{ox}) - h(\omega,R,C,C_{ox})}{h(\omega,R,C,C_{ox})} = \frac{h(aC)}{h(C)} - 1$$

$$= \frac{\{(R^2\omega^2(C+C_{ox})^2+1)(R^2\omega^2 aC(aC+C_{ox})+1)\}}{\{(R^2\omega^2 C(C+C_{ox})+1)(R^2\omega^2(aC+C_{ox})^2+1)\}} - 1 \qquad (5\text{-}12)$$

Now this equation is the frequency dependence of the signal,

$$\frac{\partial S}{\partial \omega} = \frac{2\omega R^2 C C_{ox}[X((\omega R)^2)^2 + 2Y(\omega R)^2 - (1-a)]}{\{(R^2\omega^2 C(C+C_{ox})+1)(R^2\omega^2(aC+C_{ox})^2+1)\}^2} \qquad (5\text{-}13)$$

where

$$X = a(1-a^3)C^4 + (1-a^2)(1+3a+a^2)C^3 C_{ox}$$
$$+ 3(1-a)(1+a)^2 C^2 {C_{ox}}^2 + 3(1-a^2) C {C_{ox}}^3 + (1-a){C_{ox}}^4$$
$$Y = a(1-a)C^2 + (1-a^2)CC_{ox} + (1-a){C_{ox}}^2$$

In 0 < a < 1, both X and Y are positive. The condition of $\frac{\partial S}{\partial \omega} = 0$ is

$$\omega_0 = \frac{1}{R}\sqrt{\frac{-Y+\sqrt{Y^2+X(1-a)}}{X}} \qquad (\omega_0 > 0) \qquad (5\text{-}14)$$

S will have a maximum at ω_0, generating a positive signal peak, and ω_0 is inversely proportional to R. This reveals that ω_0 will increase with ionic strength, which corresponds to a decrease in resistance. Interestingly, R to maximize S is

$$R = \frac{1}{\omega_0}\sqrt{\frac{-Y+\sqrt{Y^2+X(1-a)}}{X}} \qquad (R > 0) \qquad (5\text{-}15)$$

due to the symmetry between R and ω. Therefore, increasing ionic strength (decreasing R) will decrease the signal S in constant ω.

In summary, this qualitative analysis reveals the following three important points. First, antigen binding will induce positive signal changes in the NWFET biosensor. Second, the signal

will have a peak at a particular frequency ω_0 and increase with ionic strength. Lastly, increasing ionic strength will decrease the signal

5-4. Conclusion and prospects

A kinked semiconductor nanowire synthesized through modulation of morphology and dopants has been developed into a novel FET-based biosensor, which has the potential to be implemented as an in-vivo or point-of-care bioprobe. We have successfully demonstrated electrochemical detection in a low ionic strength solution by an n-type kinked NWFET biosensor in a microfluidic system, and verified the results by an ELISA method including SEM and TEM analysis. Furthermore, qualitative analysis of an NWFET biosensor in electrolyte with equivalent circuit guides to the high-frequency measurement enables detection of impedance changes in the system due to the association and dissociation of target biomolecules. These results and analysis constitute significant progress toward a novel NWFET bioprobe for an intracellular biosensor.

Bibliography

1 Cui, Y., Wei, Q., Park, H. & Lieber, C. M. Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species. *Science* **293**, 1289-1292 (2001).

2 Patolsky, F., Zheng, G., Hayden, O., Lakadamyali, M., Zhuang, X. & Lieber, C. M. Electrical detection of single viruses. *Proc. Natl. Acad. Sci. USA* **101**, 14017-14022 (2004).

3 Zheng, G., Patolsky, F., Cui, Y., Wang, W. U. & Lieber, C. M. Multiplexed electrical detection of cancer markers with nanowire sensor arrays. *Nature Biotechnol.* **23**, 1294-1301 (2005).

4 Ligler, F. S & Taitt, C. R. *Optical Biosensors: Today and Tomorrow*. (Elsevier Science, 2008).

5 Dey, D., & Goswami, T. Optical biosensors: A revolution towards quantum nanoscale electronics device fabrication. *J. Biomed. Biotechnol.* **348218** (2011).

6 Miyake, M. & Kurihara. K. Resting potential of the mouse neuroblastoma cells: II. Significant contribution of the surface potential to the resting potential of the cells under physiological conditions. *BBA-Mol. Cell. Res*. **762**, 256-264 (1983).

7 Tian, B., Xie, P., Kempa, T. J., Bell, D. C. & Lieber, C. M. Single crystalline kinked semiconductor nanowire superstructures. *Nature Nanotechnol*. **4**, 824-829 (2009).

8 Tian, B., Cohen-Karni, T., Qing, Q., Duan, X., Xie, P., & Lieber, C. M. Three-dimensional, flexible nanoscale field-effect transistors as localized bioprobes. *Science* **329**, 831-834 (2010).

9 Xu, L., Jiang, Z., Qing, Q., Mai, L., Zhang, Q. & Lieber, C. M. Design and synthesis of diverse functional kinked nanowire structures for nanoelectronic bioprobes. *Nano Lett*. **13**, 746-751 (2013).

10 Whitesides, G. M. The origins and the future of microfluidics. *Nature* **442**, 368-373 (2006).

11 Fainman, Y., Lee, L., Psaltis, D. & Yang, C. *Optofluidics: Fundamentals, Devices, and Applications (Biophotonics).* (McGraw-Hill Professional, 2009).

12 Gervais, T., El-Ali, J., Günther, A. & Jensen, K. F. Flow-induced deformation of shallow microfluidic channels. *Lab. Chip*. **6**, 500–507 (2006).

13 Franssila, S. *Introduction to Microfabrication*. (Wiley, 2010).

14 *About Lock-In Amplifier*, available at www.thinksrs.com

15 Kumar, A., Mukherjee, P., Guha, A., Adyantaya, S. D., Mandale, A. B., Kumar, R. & Sastry, M. Amphoterization of colloidal gold particles by capping with valine molecules and their phase transfer from water to toluene by electrostatic coordination with fatty amine molecules. *Langmuir* **16**, 9775-9783 (2000).

16 Harlow, E. & Lane, D. *Using Antibodies: A Laboratory Manual.* (Cold Spring Harbor Laboratory Press, 1999).

17 Debye, P. & Hückel, E. Zur Theorie der Elektrolyte. I. Gefrierpunktserniedrigung und verwandte Erscheinungen [The theory of electrolytes. I. Lowering of freezing point and related phenomena]. *Physikalische Zeitschrift* **24**, 185–206 (1923).

18 Stern, E., Wagner, R., Sigworth, F. J., Breaker, R., Fahmy, T. M. & Reed, M. A. Importance of the Debye screening length on nanowire field effect transistor sensors. *Nano Lett.* **7**, 3405–3409 (2007).

19 Park, S. & Yoo, J. Electrochemical Impedance Spectroscopy for Better Electrochemical Measurements. *Anal. Chem*. **75**, 455A–461A (2003).

20 Venkatraman, V. L., Zhang, F., Evans, D., Ulrich, B. & Prasad, S. Iridium oxide nanomonitors for real-time health monitoring systems. *J. Lab. Automation* **14**, 400-406 (2009).

21 Davis, J. A., James, R. O., Leckie, J. O. Surface ionization and complexation at the oxide/water interface: I. Computation of electrical double layer properties in simple electrolytes. *J. Colloid. Interf. Sci.* **63**, 480-499 (1978)

22 Manickam, A., Chevalier, A., McDermott, M., Ellington, A. D. & Hassibi, A. A CMOS Electrochemical impedance spectroscopy (EIS) biosensor array. *IEEE T. Bio-Med. Circuits. Syst.* **4**, 379-390 (2010).

23 Bard, A. J. & Faulkner, L. R. *Electrochemical methods: Fundamentals and applications.* (Wiley, 2000).

24 Schutz, C. N. & Warshel, A. What are the dielectric "constants" of proteins and how to validate electrostatic models? *PROTEINS: Structure, function, and genetics.* **44**, 400–417 (2001).

Appendix A: Atomic layer deposition

Atomic layer deposition (ALD) is one chemical deposition technique to deposit thin films of materials. Unlike conventional chemical vapor deposition (CVD), the ALD has the unique advantages of conformal deposition, atomic-scale film thickness control by self-limiting reactions, and accessibility to a diverse set of deposition materials.[1]

ALD consists of four steps. To initiate the deposition, the substrate is exposed to the first precursor which adsorbs on the surface. Once the absorption of the precursor is saturated, it forms a monolayer and un-reacted precursors are purged out of the reaction chamber via vacuum pump. Subsequently, the second precursor is introduced to the surface and reacts with the functional groups on the first layer to form a monolayer of the desired deposition compound. After excess un-reacted precursors are purged from the chamber, the first precursor is delivered again and the cycle is repeated to deposit additional monolayers. Fig A-1 describes an Al_2O_3 deposition as an example of ALD process.

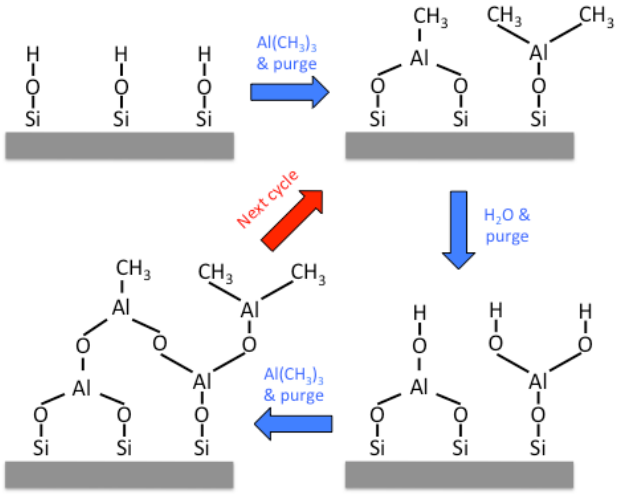


Figure A-1

Figure A-1 (Continued)

Figure A-1 Schematic of an ALD process for Al_2O_3 deposition.

To grow $Al_2O_3/ZrO_2/Al_2O_3$ dielectric multishells on semiconductor nanowire cores, the following ALD procedure is used. The device substrate with Ge/Si NWs and source/drain contacts was loaded in the ALD chamber (Savannah-100, Cambridge NanoTech) and heated to 200^{o}C. Trimethyl aluminum [$Al(CH_3)_3$, TMA], tetrakis(dimethylamino)zirconium {$Zr[N(CH_3)_2]_4$} and water were used as precursors.[2,3] Each Al_2O_3 deposition cycle consisted of 0.015s water vapor pulse, 8s N_2 purge, 0.015s TMA pulse and 8s N_2 purge. Each ZrO_2 deposition cycle consisted of 0.015s water vapor pulse, 10s N_2 purge, 0.25s Zr-precursor pulse and 15s N_2 purge. To form the charge-trapping dielectric structure shown in Fig. 3-12, a deposition sequence of 25 cycles Al_2O_3, 55 cycles ZrO_2, and 55 cycles Al_2O_3 was used.

Bibliography

1 Pinna, N. & Knez, M. *Atomic layer deposition of nanostructured materials.* (Wiley-VCH, 2011)

2 Puurunen, R. L. Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process. *J. Appl. Phys.* **97**, 121301 (2005).

3 Hausmann, D. M., Kim, E., Becker, J. & Gordon, R. G. Atomic layer deposition of hafnium and zirconium oxides using metal amide precursors. *Chem. Mater.* **14**, 4350-4358 (2002).

Appendix B: Multi-channel measurement system for programming and characterization of nanowire logic circuits

Multi-channel measurement system

Device chips were mounted in a probe station (Model 12561B, Cascade Microtech, Fig. B-1) with its back-plane grounded. A custom-designed 96-pin probe-card (Accuprobe, Fig. B-1) equipped with a BNC interface was used to electrically access the devices in the array. Measurements were made with a computer-controlled analog I/O system (PXI-6723, 3x PXIe-6124 in a PXIe-1065 chassis, National Instruments) that provided 32 channel analog-voltage generation and 12 channel analog-voltage recording. Each analog-voltage recording channel has >100 GΩ input resistance which is over 10^4 larger than the resistance of NWFETs (≤1 MΩ) and passive load resistors (≤10 MΩ) used in the circuits. To record the voltage outputs from the circuits, we connected external resistors (≤10 MΩ metal film resistors with ±1% tolerance, Vishay Dale) to the drain of individual NW devices in the NW logic tile and monitored output voltage at the drain electrode (Fig. B-1). The value of the external resistors was chosen to be at least one order of magnitude larger than the 'on' state resistance of active nodes. The passive resistor loads used in our circuit prevented us from achieving full-swing operation, although future integration of complementary NWFET loads[1] could minimize this effect. Simplified

circuit schemes excluding resistor connections were presented in Figs. 3-3, 3-8, 3-9, 3-10, and 3-11.

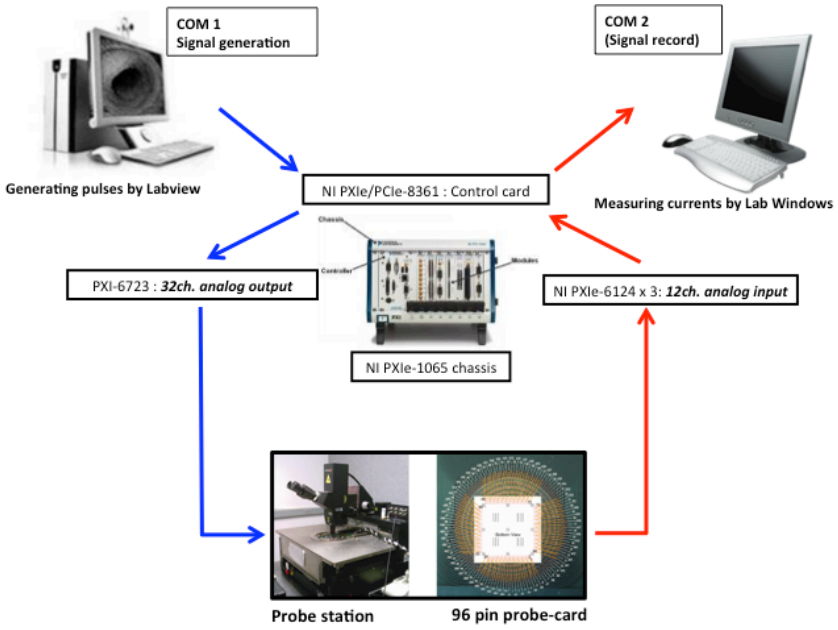


Figure B-1 Schematic of the multi-channel I/O system. Blue and red arrows indicate input and output flow of data and command.

Node Programming

We applied the "1/3 rule"[2] to modulate nodes to be set or reset without cross-talk between adjacent nodes. Fig. B-2 shows three NWs (NW1-NW3) in block-1 (left pink dashed box) and two NWs (NW4-NW5) in block-2 (right pink dashed box), both with three top-gates (grey). The two blocks are connected by external wiring (black lines with arrows) before programming. For each step, the voltages applied to the source/drain electrodes of the NWs

(V_{NW}) and the top-gates (V_{TG}) are marked beside their corresponding terminals. A typical value of the programming voltage, V, is -6 V. The voltage drop across the charge-trapping dielectric, Vgs, is defined as V_{TG}-V_{NW}, and is presented by colored dots as explained in detail below. All nodes are first set to inactive by setting Vgs to –V (brown dots). The active node on NW2 in block-1 is programmed by setting Vgs to V (green dot) for the target node and V/3 (yellow dots) or –V/3 (cyan dots) for all other nodes. The active node on NW4 in block-2 is programmed with a similar method as was NW2. It is noteworthy that Vgs is set to V only for the target node and is at ±V/3 for all other nodes in both blocks. The successful implementation of various logic circuits (Figs. 3-8, 3-9, 3-10, and 3-11) demonstrates that the ±V/3 Vgs does not disturb the charge-trapping states of these nodes and thus confirms the validity of this programming approach.

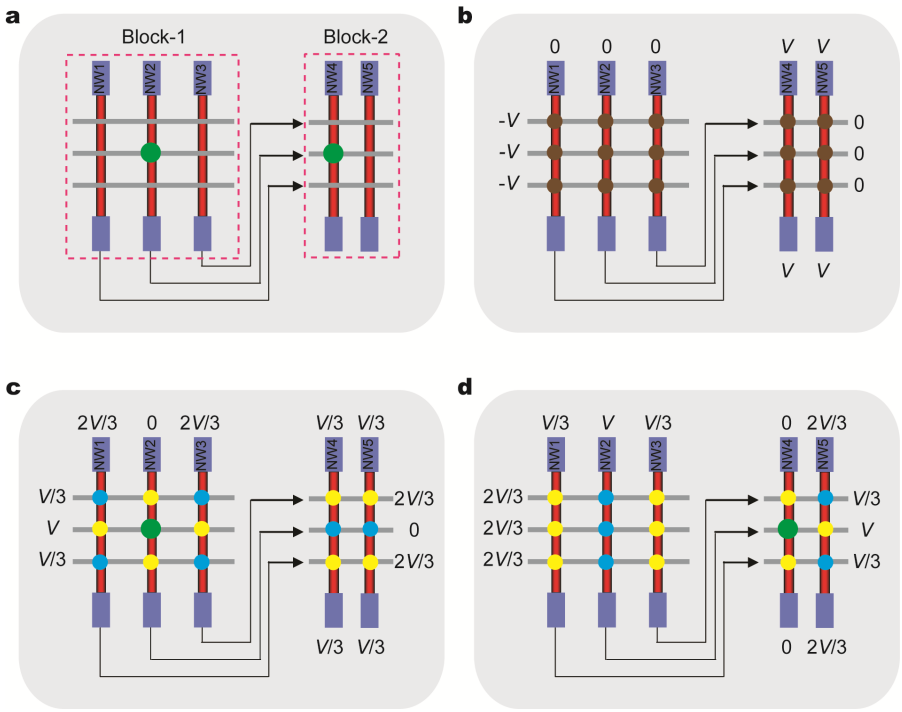


Figure B-2

Figure B-2 (Continued)

Figure B-2 Schematic of active node pattern programming using the V/3 rule. (a), Schematic of the circuit and the target active node pattern (green dots). (b)-(d) Step-by-step programming of the active node pattern shown in (a), which does not affect the state of the other adjacent nodes. Brown, green, cyan, and yellow dots indicate nodes with applied bias of –V, V, -V/3, and V/3, respectively.

Bibliography

1 Nam, S., Jiang, X. C., Xiong, Q. H., Ham, D. & Lieber, C. M. Vertically integrated, three-dimensional nanowire complementary metal-oxide-semiconductor circuits. *Proc. Nat. Acad. Sci. U. S. A.* **106**, 21035-21038 (2009).

2 Ishiwara, H. The FET-type FeRAM. *Top. Appl. Phys*. **93**, 233-251 (2004).

Appendix C : Signal artifacts in biosensing by ionic strength changes

An electrochemical biosensor can detect not only charged molecule association/dissociation on its surface but also electrical artifacts such as ionic strength changes.[1] NWFET biosensors are no exception to this. Fig. C-1 shows change in conductance of an n-type kinked NWFET in KCl solutions of various concentrations but with the same pH. The microfluidic system with low frequency electrical measurement (Vsd = 200mVpp, 79Hz), which is the same as was used in the aforementioned biosensing experiments, was used for these experiments with an Ag/AgCl reference electrode (V_{WG} = 0V). We observed an increase in conductance proportional to the concentration of KCl solution, which could be related to the reference electrode because the change in number of chloride ion (in KCl or PBS) can induce a change in the potential of the reference electrode. To analyze the result quantitatively, consider the Nernst equation,[2]

$$E = E^0 - \frac{RT}{F}\ln Q = 197mV - 59.2mV \log_{10} Q \quad at\ RT \tag{C-1}$$

where E, E^0, R, T, F, Q are reduction potential, reduction potential of Ag/AgCl saturated by KCl, ideal gas constant, absolute temperature, Faraday constant, and reaction quotient. If the concentration of Cl^- is increased by a factor of two, the potential change ΔE is

$$\Delta E = 59.2mV \log_{10} Q + 59.2mV \log_{10} 2Q = 17.8\,mV \tag{C-2}$$

This value corresponds to the results in Fig. C-1.

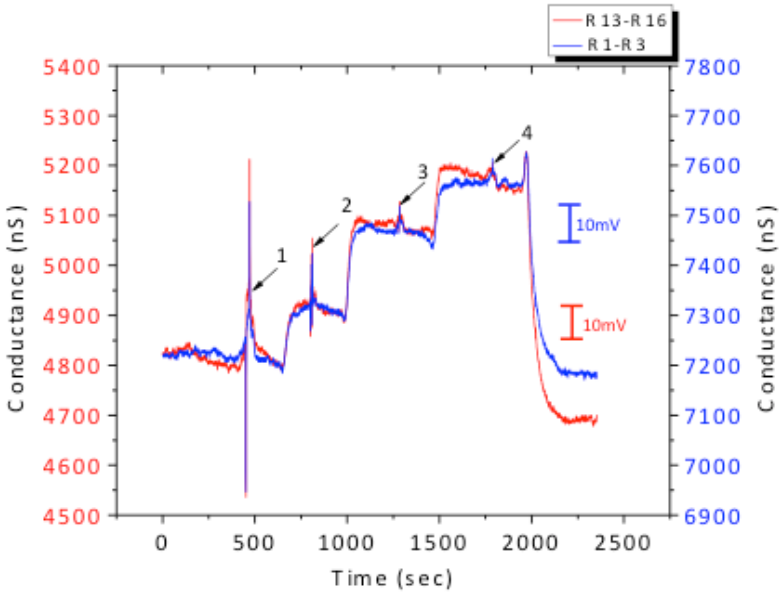


Figure C-1 Conductance vs. time curves of n-type kinked NWFETs in different ionic strength solutions. The trace is initially recorded with the devices in 87.4 μM KCl solution (pH 6.2). The four black arrows indicate the time at which we began flowing 175 μM, 350 μM, 700 μM, and 87.4 μM KCl solutions with the same pH (pH 6.2).

To clarify artifacts from ionic strength changes in biosensing experiments, we employed a dual reference electrode (Ag/AgCl) setup to measure the potential change between them as a function of ionic strength as determined by various ions and proteins. Fig. C-2a shows the setup with microfluidic flow channels. The DC potential change between the two electrodes when flowing 100nM PSA in PBS 1mX with and without an ultrafitration/dialysis protein filtration process is shown in Fig. C-2b. It should be noted that the buffer which contains the PSA is PBS 1X; thus, even adding ~1μL of the 1X protein solution to PBS 1mX could significantly change the ionic strength of the original buffer solution. Understood in the context of the results in Fig.

C-1, the DC shifts in Fig. C-2b are the effect of not proteins but rather ionic strength change during mixing the PBS 1X/protein solution with PBS 1mX buffer. Therefore, removing the high ionic background buffer of proteins is critical to performing appropriate biosensing experiments.

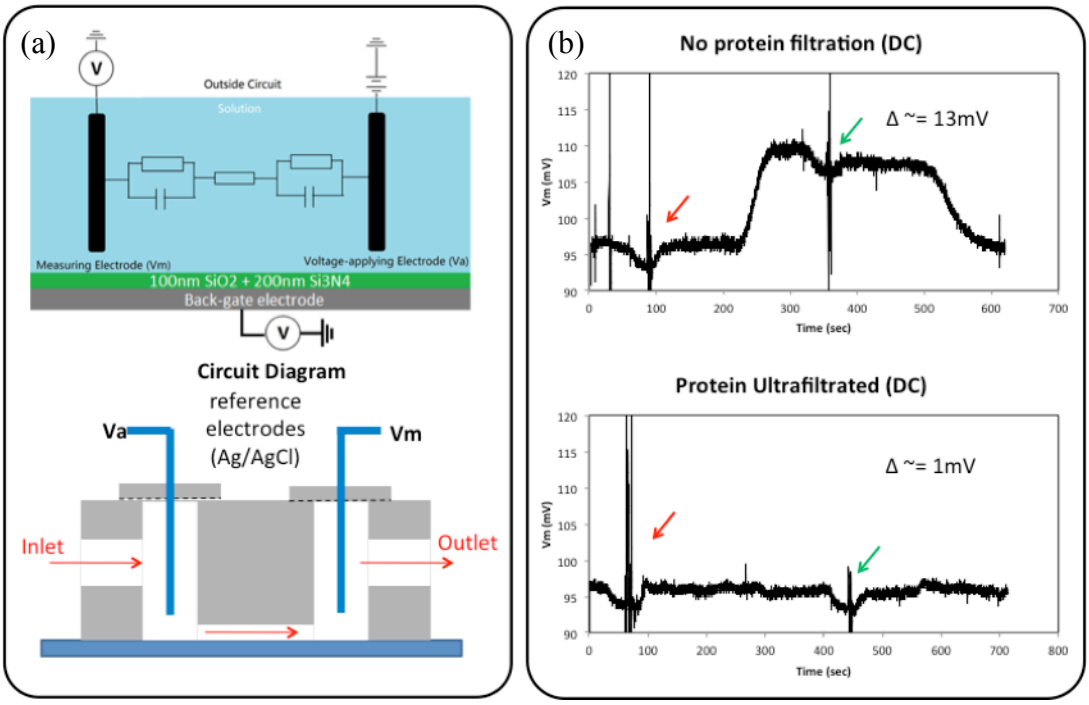


Figure C-2 Dual Ag/AgCl electrode microfluidic setup and the potential changes between them induced by flow of filtered and unfiltered protein samples. (a) Equivalent circuits (top) and schematic of side view of the dual electrode setup in a microfluidic chamber (bottom). (b) The potential change between the electrodes upon the introduction of filtered (top) and unfiltered (bottom) 100nM PSA in PBS 1mX. Note that PSA buffer solution is PBS 1X before the filtration process. Red and green arrows indicate the time at which we began flowing protein samples and rinsing out respectively.

Bibliography

1 Tarasov, A., Wipf, M., Stoop, R. L., Bedner, K., Fu, W., Guzenko, V. A., Knopfmacher, O., Calame, M. and Schönenberger, C. Understanding the electrolyte background for biochemical sensing with ion-sensitive field-effect transistors. *ACS Nano* **6**, 9291–9298 (2012).

2 Stock, J. T. & Orna, M. V. *Electrochemistry, past and present.* (American Chemical Society, 1989).